

RF430FRL15xH NFC ISO 15693 Sensor Transponder

1 Device Overview

1.1 Features

- ISO/IEC 15693, ISO/IEC 18000-3 (Mode 1) Compliant RF Interface
- Power Supply System With Either Battery or 13.56-MHz H-Field Supply
- 14-Bit Sigma-Delta Analog-to-Digital Converter (ADC)
- Internal Temperature Sensor
- Resistive Sensor Bias Interface
- CRC16 CCITT Generator
- MSP430™ Mixed-Signal Microcontroller
 - 2KB of FRAM
 - 4KB of SRAM
 - 8KB of ROM
 - Supply Voltage Range: 1.45 V to 1.65 V
 - Low Power Consumption
 - Active Mode (AM): 140 μ A/MHz (1.5 V)
 - Standby Mode (LPM3): 16 μ A
 - 16-Bit RISC Architecture
 - Up to 2-MHz CPU System Clock
 - Compact Clock System
 - 4-MHz High-Frequency Clock
 - 256-kHz Internal Low-Frequency Clock Source
- External Clock Input
- 16-Bit Timer_A With Three Capture/Compare Registers
- LV Port Logic
 - V_{OL} Lower Than 0.15 V at 400 μ A
 - V_{OH} Higher Than ($V_{DDB} - 0.15$ V) at 400 μ A
 - Timer_A PWM Signal Available on All Ports
- eUSCI_B Module Supports 3-Wire and 4-Wire SPI and I²C
- 32-Bit Watchdog Timer (WDT_A)
- ROM Development Mode (Map ROM Addresses to SRAM to Enable Firmware Development)
- Full 4-Wire JTAG Debug Interface
- For Complete Module Descriptions, See the *RF430FRL15xH Family Technical Reference Manual* ([SLAU506](#))
- For Application Operation and Programming, See the *RF430FRL15xH Firmware User's Guide* ([SLAU603](#))

1.2 Applications

- Industrial Wireless Sensors
- Medical Wireless Sensors

1.3 Description

The RF430FRL15xH device is a 13.56-MHz transponder chip with a programmable 16-bit MSP430™ low-power microcontroller. The device features embedded universal FRAM nonvolatile memory for storage of program code or user data such as calibration and measurement data. The RF430FRL15xH supports communication, parameter setting, and configuration through the ISO/IEC 15693, ISO/IEC 18000-3 compliant RFID interface and the SPI or I²C interface. Sensor measurements are supported by the internal temperature sensor and the onboard 14-bit sigma-delta analog-to-digital converter (ADC), and digital sensors can be connected through SPI or I²C.

The RF430FRL15xH device is optimized for operation in fully passive (battery-less) or single-cell battery-powered (semi-active) mode to achieve extended battery life in portable and wireless sensing applications. FRAM is a nonvolatile memory that combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash, all at lower total power consumption.



Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE ⁽²⁾ |
|--------------|-----------|--------------------------|
| RF430FRL152H | VQFN (24) | 4 mm x 4 mm |
| RF430FRL153H | VQFN (24) | 4 mm x 4 mm |
| RF430FRL154H | VQFN (24) | 4 mm x 4 mm |

- (1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 9, or see the TI web site at www.ti.com.
- (2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in Section 9.

1.4 Functional Block Diagram

Figure 1-1 shows the block diagram of the RF430FRL15xH device.

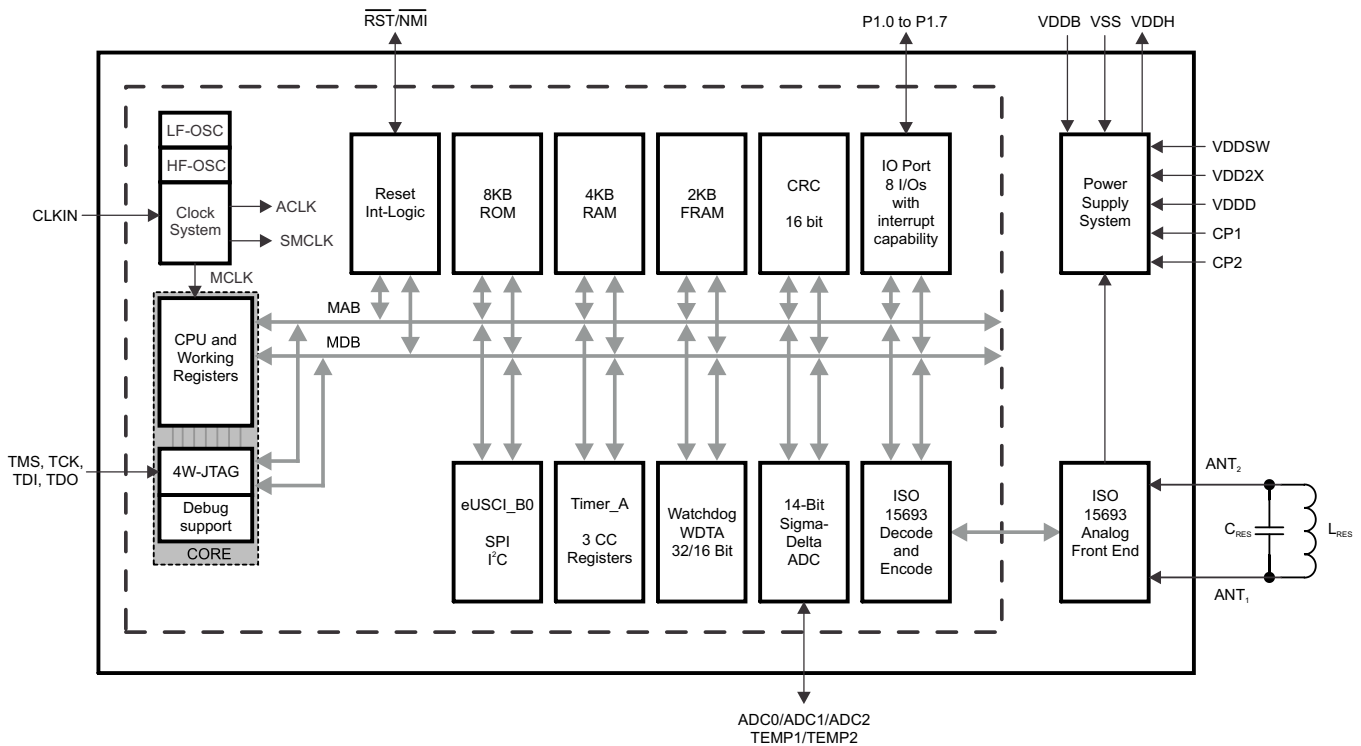


Figure 1-1. Functional Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from November 13, 2014 to December 8, 2014 | Page |
|---|-------------|
| • Corrected all instances of the title of the <i>RF430FRL15xH Family Technical Reference Manual</i> | <u>1</u> |
| • Corrected all instances of the title of the <i>RF430FRL15xH Firmware User's Guide</i> | <u>1</u> |
| • Moved T_{stg} to <i>Absolute Maximum Ratings</i> table | <u>10</u> |
| • Changed title of Section 5.2 to <i>ESD Ratings</i> | <u>10</u> |

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison⁽¹⁾

| Device | FRAM (KB) | SRAM (KB) | Timer | 13.56-MHz ISO/IEC 15693 Front End | eUSCI_B | SD14 |
|--------------|-----------|-----------|-------|-----------------------------------|---------|------|
| RF430FRL152H | 2 | 4 | Yes | Yes | Yes | Yes |
| RF430FRL153H | 2 | 4 | Yes | Yes | No | Yes |
| RF430FRL154H | 2 | 4 | Yes | Yes | Yes | No |

(1) For the most current part, package, and ordering information for all available devices, see the *Package Option Addendum* in Section 9, or see the TI web site at www.ti.com.

4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pin assignments on the 24-pin RGE package.

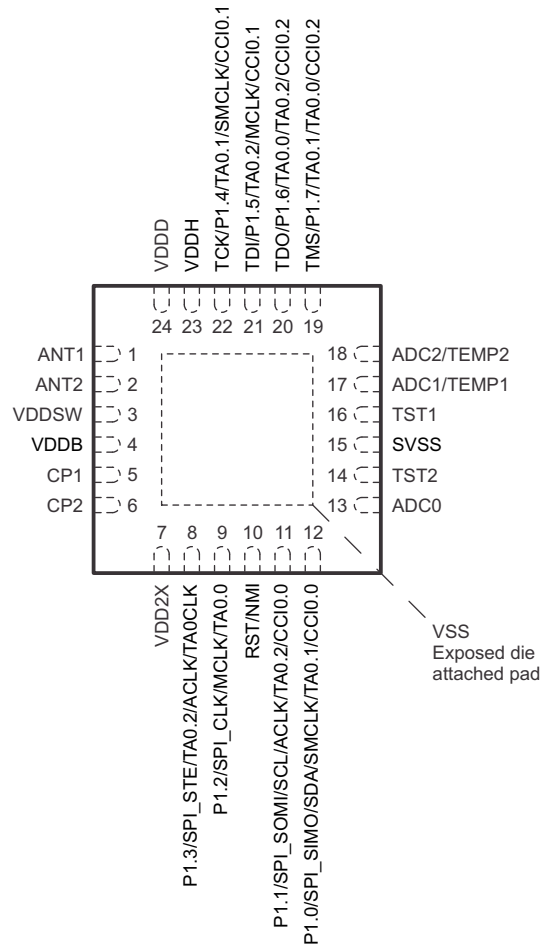


Figure 4-1. 24-Pin RGE Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals.

Table 4-1. Signal Descriptions

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|---|-----|--------------------|--|
| NAME | NO. | | |
| ANT1 | 1 | I | Antenna input 1 |
| ANT2 | 2 | I | Antenna input 2 |
| V _{DDSW} | 3 | | Switched supply voltage |
| V _{DDB} | 4 | | Battery supply voltage |
| CP1 | 5 | | Charge pump flying cap terminal 1 |
| CP2 | 6 | | Charge pump flying cap terminal 2 |
| V _{DD2X} | 7 | | Voltage doubler output |
| P1.3 SPI_STE TA0.2 ACLK TA0CLK | 8 | I/O | General-purpose digital I/O SPI slave transmit enable Timer_A TA0 OUT2 output ACLK output (divided by 1, 2, 4, 8, 16, or 32) Timer_A TA0 clock signal TA0CLK input |
| P1.2 SPI_CLK MCLK TA0.0 | 9 | I/O | General-purpose digital I/O SPI clock MCLK output Timer_A TA0 OUT0 output |
| RST/NMI | 10 | I | Reset input active low Non-maskable interrupt input |
| P1.1 SPI_SOMI SCL ACLK TA0.2 CCI0.0 | 11 | I/O | General-purpose digital I/O SPI slave out master in I ² C clock ACLK output (divided by 1, 2, 4, or 8) Timer_A TA0 OUT2 output Timer_A TA0 CCR0 capture: CCI0B input, compare |
| P1.0 SPI_SIMO SDA SMCLK TA0.1 CCI0.0 | 12 | I/O | General-purpose digital I/O SPI slave in master out I ² C data SMCLK output Timer0_A3 OUT1 output Timer_A TA0 CCR0 capture: CCI0A input, compare |
| ADC0 | 13 | I | ADC input pin 0 |
| TST2 | 14 | | Internal; connect to GND |
| SVSS | 15 | | Sensor reference potential |
| TST1 | 16 | | Internal; connect to GND |
| ADC1 / TEMP1 | 17 | | ADC input pin 1 / Resistive bias pin 1 |
| ADC2 / TEMP2 | 18 | | ADC input pin 2 / Resistive bias pin 2 |

(1) I = input, O = output

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | I/O ⁽¹⁾ | DESCRIPTION |
|--|-----|--------------------|---|
| NAME | NO. | | |
| TMS P1.7 TA0.1 TA0.0 CCI0.2 | 19 | I/O | JTAG test mode select General-purpose digital I/O Timer_A TA0 OUT1 output Timer_A TA0 OUT0 output Timer_A TA0 CCR2 capture: CCI2B input, compare |
| TDO P1.6 TA0.0 TA0.2 CCI0.2 | 20 | I/O | JTAG test data output General-purpose digital I/O Timer_A TA0 OUT0 output Timer_A TA0 OUT2 output Timer_A TA0 CCR2 capture: CCI2A input, compare |
| TDI P1.5 TA0.2 MCLK CCI0.1 | 21 | I/O | JTAG test data input General-purpose digital I/O Timer_A TA0 OUT2 output MCLK output Timer_A TA0 CCR1 capture: CCI1B input, compare |
| TCK P1.4 TA0.1 SMCLK CCI0.1 CLKIN | 22 | I/O | JTAG test clock General-purpose digital I/O Timer_A TA0 OUT1 output SMCLK output Timer_A TA0 CCR1 capture: CCI1A input, compare External clock input pin |
| V _{DDH} | 23 | O | Rectified voltage from RF-AFE |
| V _{DDD} | 24 | | Digital supply voltage |
| V _{SS} | Pad | | Ground reference, bonded to exposed pad ⁽²⁾ |

(2) VSS combines both digital ground (DV_{SS}) and analog ground (AV_{SS})

4.3 Pin Multiplexing

The GPIO port pins are multiplexed with other functions including analog peripherals and serial communication modules. The pin functions are selected by a combination of register values and device modes. For schematics of the port pins and details of the multiplexing for each, refer to [Section 6.7](#).

4.4 Connections for Unused Pins

The correct termination of all unused pins is listed in [Table 4-2](#).

Table 4-2. Connection of Unused Pins

| Pin | Potential | Comment |
|------------------------------------|----------------------|---|
| TDI/TMS/TCK | Open | When used for JTAG function |
| $\overline{\text{RST}}/\text{NMI}$ | V_{CC} or V_{SS} | 10-nF capacitor to GND/ V_{SS} |
| Px.0 to Px.7 | Open | Set to port function, output direction |
| TDO | Open | Convention: leave TDO terminal as JTAG function |

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|------|-----------------|------|
| Voltage applied at V_{DDB} referenced to V_{SS} (V_{AMR}) | -0.3 | 1.65 | V |
| Voltage applied at V_{ANT} referenced to V_{SS} (V_{AMR}) | -0.3 | 3.6 | V |
| Voltage applied to any pin (references to V_{SS}) | -0.3 | $V_{DDB} + 0.3$ | V |
| Diode current at any device pin ⁽²⁾ | | ± 2 | mA |
| Current derating factor when I/O ports are switched in parallel electrically and logically ⁽³⁾ | | 0.9 | |
| Storage temperature range, T_{stg} ^{(4) (5) (6)} | -40 | 125 | °C |

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are referenced to V_{SS} .
- The diode current increases to ± 4.5 mA when two pins are connected, it increases to ± 6.75 mA when three pins are connected, and so on.
- Soldering during board manufacturing must follow the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels. If hand soldering is required for application prototyping, peak temperature must not exceed 250°C for a total of 5 minutes for any single device.
- Data retention on FRAM memory cannot be ensured when exceeding the specified maximum storage temperature, T_{stg} .
- Programming of devices with user application code should only be performed after reflow or hand soldering. Factory programmed information, such as calibration values, are designed to withstand the temperatures reached in the current JEDEC J-STD-020 specification.

5.2 ESD Ratings

| | VALUE | UNIT |
|---|---|-----------------|
| V_{ESD} Electrostatic discharge (ESD) performance | Human body model (HBM), per ANSI/ESDA/JEDEC JS001 ⁽¹⁾⁽²⁾ | ± 2000 V |

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- Low leakage pin: ADC0 has reduced ESD tolerance of ± 500 V HBM.

5.3 Recommended Operating Conditions

Typical data are based on $V_{DDB} = 1.5$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|--|------|-----|------|---------------|
| V_{DDB} Supply voltage during program execution | 1.45 | | 1.65 | V |
| V_{SS} Supply voltage (GND reference) | | 0 | | V |
| T_A Operating free-air temperature | 0 | | 70 | °C |
| C_{VDDB} Capacitor on V_{DDB} ⁽¹⁾ | | 100 | | nF |
| C_{VDDSW} Capacitor on V_{DDB} ⁽¹⁾ | | 2.2 | | μF |
| C_{FLY} Charge pump capacitor between CP1 and CP2. Recommended ratio between C_{FLY} and C_{VDD2X} is $\geq 1:10$. ⁽¹⁾ | | 10 | | nF |
| C_{VDD2X} Capacitor on V_{DD2X} . Recommended ratio between C_{FLY} and C_{VDD2X} is $\geq 1:10$. ⁽¹⁾ | | 100 | | nF |
| C_{VDDD} Capacitor on V_{DDD} ⁽¹⁾ | | 1 | | μF |
| C_{SVSS} Capacitor between $SVSS$ and V_{SS} ⁽¹⁾ | | 1 | | μF |
| f_{SYSTEM} System frequency ^{(2) (3)} | | | 2 | MHz |
| f_{CLKIN} External clock input frequency | | | 32 | kHz |

- Low equivalent series resistance (ESR) capacitor
- The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
- Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.

5.4 Recommended Operating Conditions, Resonant Circuit

| | | MIN | NOM | MAX | UNIT |
|-----------------|-------------------------|-----|-----------------------|-----|------------|
| f_c | Carrier frequency | | 13.56 | | MHz |
| V_{ANT_peak} | Antenna input voltage | | | 3.6 | V |
| Z | Impedance of LC circuit | 6.5 | 15.5 | | k Ω |
| L_{RES} | Coil inductance | | 2.66 | | μ H |
| C_{RES} | Resonance capacitance | | $51.8 - C_{IN}^{(1)}$ | | pF |
| QT | Tank quality factor | | 30 | | |

(1) See the RF13M parameter section.

5.5 Active Mode Supply Current Into V_{DDB} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | EXECUTION MEMORY | V_{DDB} | Frequency ($f_{MCLK} = f_{SMCLK}$) | | | | UNIT |
|----------------------|------------------|-----------|--------------------------------------|-----|-------|-----|---------|
| | | | 1 MHz | | 2 MHz | | |
| | | | TYP | MAX | TYP | MAX | |
| $I_{AM, FRAM}^{(2)}$ | FRAM | 1.5 V | 330 | 420 | 480 | 580 | μ A |
| $I_{AM, RAM}^{(2)}$ | RAM | 1.5 V | 220 | 300 | 250 | 320 | μ A |
| $I_{AM, ROM}^{(2)}$ | ROM | 1.5 V | 220 | 300 | 230 | 300 | μ A |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) $f_{ACLK} = 256$ kHz, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0

5.6 Low-Power Mode Supply Current (Into V_{DDB}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | V_{DDB} | 0°C | | 20°C | | 45°C | | 70°C | | UNIT |
|------------------|---|-----|-----|------|-----|------|-----|------|-----|---------|
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0}^{(2)}$ | $f_{MCLK} = \text{off}, f_{SMCLK} = 1$ MHz, $f_{ACLK} = 32$ kHz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 | 170 | 230 | 190 | | 210 | | 260 | 340 | μ A |
| $I_{LPM3}^{(3)}$ | $f_{MCLK} = f_{SMCLK} = \text{off}, f_{ACLK} = 16$ kHz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 | 12 | 20 | 13 | | 16 | | 25 | 65 | μ A |
| $I_{LPM4}^{(4)}$ | $f_{MCLK} = f_{SMCLK} = f_{ACLK} = 0$ Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 | 11 | 16 | 12 | | 15 | | 24 | 60 | μ A |

(1) Including current for WDT clocked by ACLK.

(2) CSS: SELM=SELS=HF_CLK, SELA=LF_CLK, DIVM=/2 (2MHz), DIVS=/4 (1MHz), DIVA=/8 (32kHz)
SD14: reset values

RFPMM: battery switch on (EN_BATSWITCH=1)

(3) CSS: SELM=HF_CLK, SELS=SELA=LF_CLK, DIVM=/2 (2MHz), DIVS=/32 (8kHz), DIVA=/16 (16kHz)

SD14: reset values

RFPMM: EN_BATSWITCH=1 (battery switch enabled)

(4) CSS: SELM=HF_CLK, SELS=SELA=LF_CLK, DIVM=/2 (2MHz), DIVS=/32 (8kHz), DIVA=/16 (16kHz)

SD14: reset values

RFPMM: EN_BATSWITCH=1 (battery switch enabled)

5.7 Digital I/Os (P1, RST/NMI)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---|--|----------------------------|-----|---------------------------|------|
| V _{OH} | High-level output voltage | V _{DDB} = 1.5 V, I _{OH} = -400 μA ⁽¹⁾ for port P1 | V _{DDB} - 0.15 | | | V |
| V _{OL} | Low-level output voltage | V _{DDB} = 1.5 V, I _{OL} = 400 μA ⁽²⁾ for port P1 | | | 0.15 | V |
| V _{IH} | High-level input voltage | V _{DDB} = 1.5 V | 0.7 × V _{DDB} | | | V |
| V _{IL} | Low-level input voltage | V _{DDB} = 1.5 V | | | 0.3 × V _{DDB} | V |
| I _{OH} | High-level output current | V _{DDB} = 1.45 V to 1.65 V for port P1 | -400 | | | μA |
| I _{OL} | Low-level output current | V _{DDB} = 1.45 V to 1.65 V for port P1 | | | 400 | μA |
| I _{LKG} | High-impedance leakage current | V _{DDB} = 1.45 V to 1.65 V | -100 | | 100 | nA |
| t _{INT} | External interrupt timing ⁽³⁾ | P1.x, V _{DDB} = 1.45 V to 1.65 V | | 200 | | ns |
| R _{PULL} | Pullup or pulldown resistor | V _{DDB} =1.5 V, For pullup: V _{IN} = V _{SS} , For pulldown: V _{IN} = V _{DDB} for port P1 | 30 | 35 | 40 | kΩ |
| R _{RST} | Pullup on RST/NMI | | 30 | 35 | 40 | kΩ |
| R _{EXT} | External pullup resistor on RST terminal (optional) | | | 47 | | kΩ |
| C _{EXT} | External capacitor on RST terminal | | | 10 | | nF |

- (1) The maximum total current I_{OH}, for all outputs combined should not exceed 500 μA to hold the maximum voltage drop specified, limited by low leakage switches.
- (2) The maximum total current I_{OL}, for all outputs combined should not exceed 500 μA to hold the maximum voltage drop specified.
- (3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_{INT} is met.

5.8 High-Frequency Oscillator (4 MHz), HFOSC

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-----------------|------|-----|------|------|
| f _{HFOSC} | ±20% | 3.04 | 3.8 | 4.56 | MHz |
| Duty cycle | | 45% | 50% | 55% | |
| t _{START} | | | 1 | | μs |

5.9 Low-Frequency Oscillator (256 kHz), LFOSC

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-----------------|-----|-----|-----|------|
| f _{LFO} | trimmed ±5% | 243 | 256 | 269 | kHz |
| Duty cycle | | 45% | 50% | 55% | |
| t _{START} | | | | 11 | μs |

5.10 Wake-Up From Low-Power Modes

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{DDB} | MIN | TYP | MAX | UNIT |
|----------------------------|--|-------------------------|------------------|-----|-----|-----|------|
| t _{WAKE-UP LPM0} | Wake-up time from LPM0 to active mode ⁽¹⁾ | | 1.5 V | | 3.2 | 6 | μs |
| t _{WAKE-UP LPM34} | Wake-up time from LPM3 or LPM4 to active mode ⁽¹⁾ | | 1.5 V | | 160 | 260 | μs |
| t _{WAKE-UP RESET} | Wake-up time from $\overline{\text{RST}}$ to active mode. ⁽²⁾ | V _{DDB} stable | 1.5 V | | 210 | 310 | μs |

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is fetched. This time includes the activation of the FRAM during wake-up. f_{MCLK} = 2 MHz.

(2) The wake-up time is measured from the rising edge of the $\overline{\text{RST}}$ signal until the first instruction of the user program is fetched. This time includes the activation of the FRAM during wake-up. f_{MCLK} = 2 MHz.

5.11 Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{DDB} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|--|------------------|-----|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10% | 1.5 V | | | 4 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 1.5 V | 20 | | | ns |

5.12 eUSCI (SPI Master Mode) Recommended Operating Conditions

| PARAMETER | | CONDITIONS | V _{DDB} | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------|---|------------------|-----|-----|---------------------|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK, ACLK Duty cycle = 50% ± 10% | 1.5 V | | | f _{SYSTEM} | MHz |

5.13 eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{DDB} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|------------------|-----|-----|-----|------------------|
| t _{STE,LEAD} | STE lead time, STE active to clock | UCSTEM = 0, UCMODEx = 01 or 10 | 1.5 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 1.5 V | 1 | | | |
| t _{STE,LAG} | STE lag time, Last clock to STE inactive | UCSTEM = 0, UCMODEx = 01 or 10 | 1.5 V | 1 | | | UCxCLK cycles |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 1.5 V | 1 | | | |
| t _{STE,ACC} | STE access time, STE active to SIMO data out | UCSTEM = 0, UCMODEx = 01 or 10 | 1.5 V | | | 55 | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 1.5 V | | | 35 | |
| t _{STE,DIS} | STE disable time, STE inactive to SIMO high impedance | UCSTEM = 0, UCMODEx = 01 or 10 | 1.5 V | | | 40 | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 1.5 V | | | 30 | |
| t _{SU,MI} | SOMI input data setup time | | 1.5 V | 35 | | | ns |
| t _{HD,MI} | SOMI input data hold time | | 1.5 V | 0 | | | ns |
| t _{VALID,MO} | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF | 1.5 V | | | 30 | ns |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | C _L = 20 pF | 1.5 V | 0 | | | ns |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO}(eUSCI) + t_{SU,SI}(Slave), t_{SU,MI}(eUSCI) + t_{VALID,SO}(Slave))$.

For the slave's parameters $t_{SU,SI}(Slave)$ and $t_{VALID,SO}(Slave)$ see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-1](#) and [Figure 5-2](#).

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in [Figure 5-1](#) and [Figure 5-2](#).

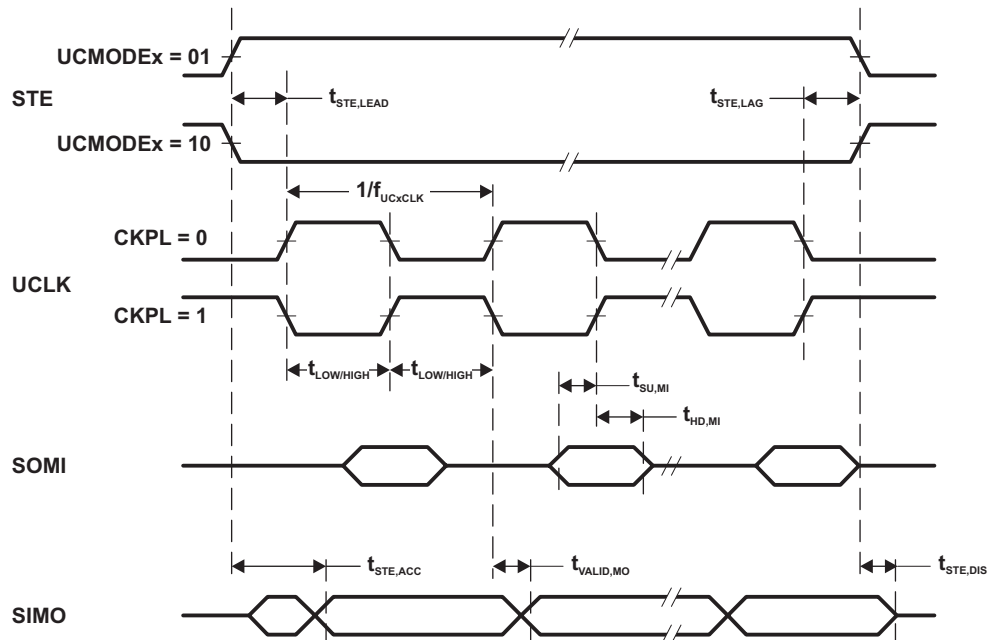


Figure 5-1. SPI Master Mode, CKPH = 0

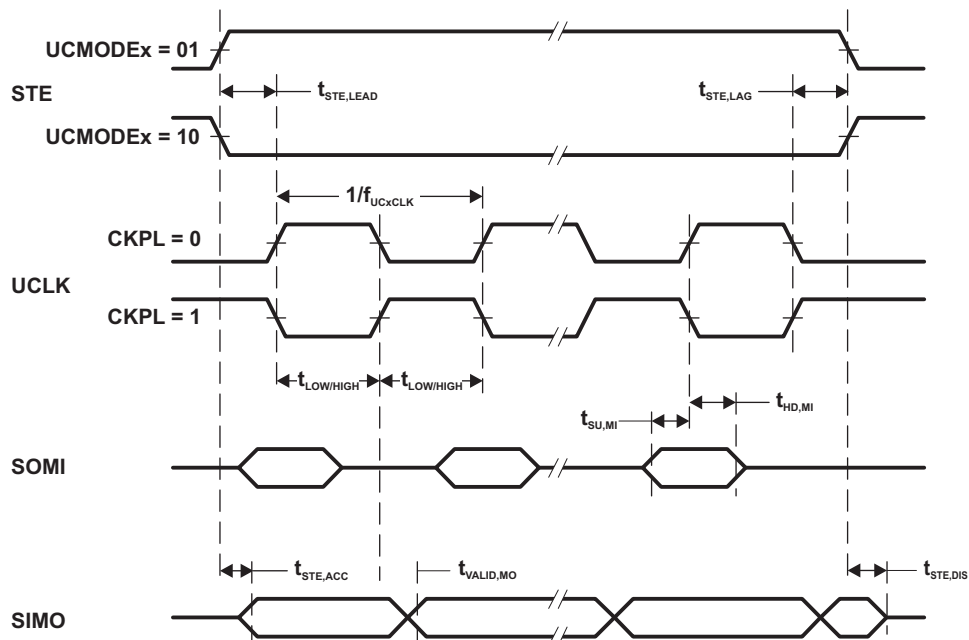


Figure 5-2. SPI Master Mode, CKPH = 1

5.14 eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{DDB} | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|------------------|-----|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE active to clock | | 1.5 V | 7 | | | ns |
| t _{STE,LAG} | STE lag time, Last clock to STE inactive | | 1.5 V | 0 | | | ns |
| t _{STE,ACC} | STE access time, STE active to SOMI data out | | 1.5 V | | | 65 | ns |
| t _{STE,DIS} | STE disable time, STE inactive to SOMI high impedance | | 1.5 V | | | 40 | ns |
| t _{SU,SI} | SIMO input data setup time | | 1.5 V | 2 | | | ns |
| t _{HD,SI} | SIMO input data hold time | | 1.5 V | 5 | | | ns |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF | 1.5 V | | | 30 | ns |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF | 1.5 V | 4 | | | ns |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.

For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-3](#) and [Figure 5-4](#).

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in [Figure 5-3](#) and [Figure 5-4](#).

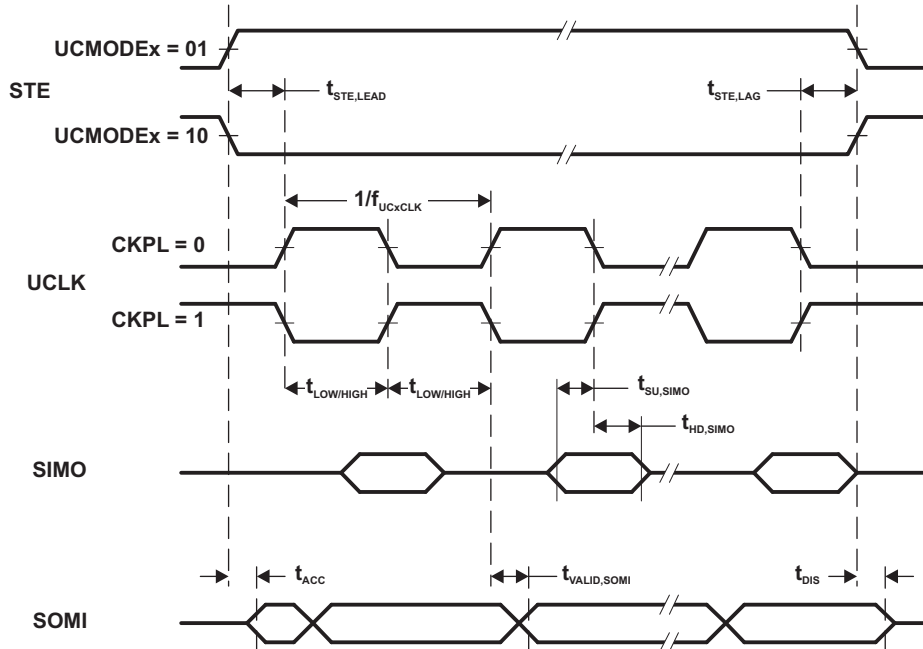


Figure 5-3. SPI Slave Mode, CKPH = 0

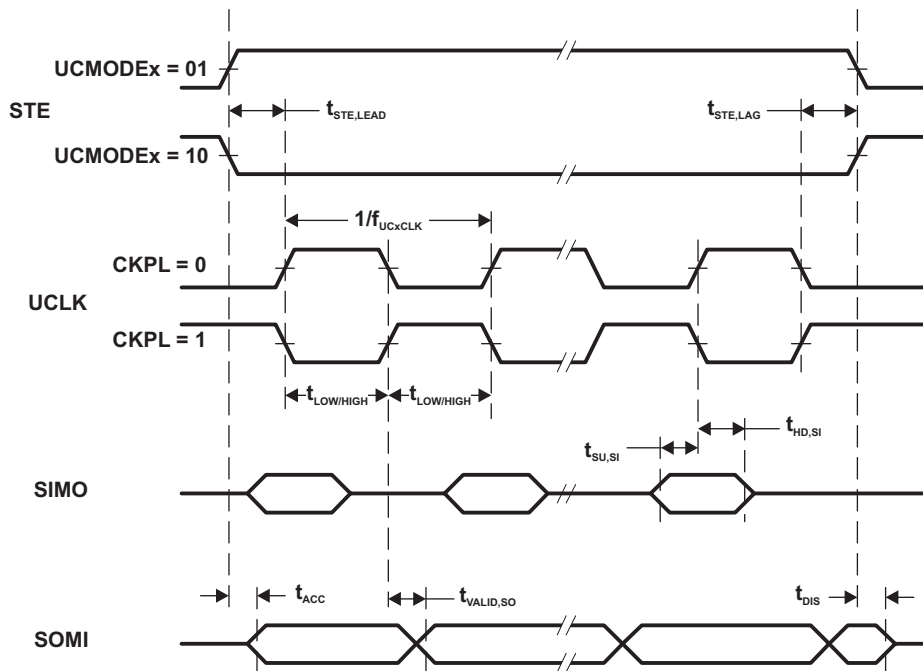


Figure 5-4. SPI Slave Mode, CKPH = 1

5.15 eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-5](#))

| PARAMETER | TEST CONDITIONS | V _{DDB} | MIN | TYP | MAX | UNIT |
|----------------------|--|------------------|-------------|---------------------|-----|------|
| f _{eUSCI} | eUSCI input clock frequency Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10% | | | f _{SYSTEM} | | MHz |
| f _{SCL} | SCL clock frequency | 1.5 V | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | 1.5 V | 4.0 | | | μs |
| | f _{SCL} > 100 kHz | | 0.6 | | | |
| t _{SU,STA} | Setup time for a repeated START | 1.5 V | 4.7 | | | μs |
| | f _{SCL} > 100 kHz | | 0.6 | | | |
| t _{HD,DAT} | Data hold time | 1.5 V | 0 | | | ns |
| t _{SU,DAT} | Data setup time | 1.5 V | 250 | | | ns |
| t _{SU,STO} | Setup time for STOP | 1.5 V | 4.0 | | | μs |
| | f _{SCL} > 100 kHz | | 0.6 | | | |
| t _{SP} | Pulse duration of spikes suppressed by input filter | 1.5 V | UCGLITx = 0 | | 600 | ns |
| | | | UCGLITx = 1 | 25 | 300 | ns |
| | | | UCGLITx = 2 | 12.5 | 150 | ns |
| | | | UCGLITx = 3 | 6.25 | 75 | ns |
| t _{TIMEOUT} | Clock low time-out | 1.5 V | UCCLTOx = 1 | 27 | | ms |
| | | | UCCLTOx = 2 | 30 | | ms |
| | | | UCCLTOx = 3 | 33 | | ms |

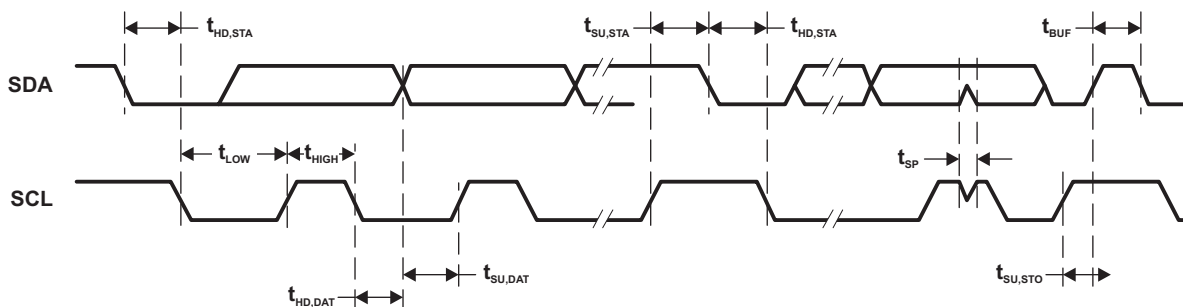


Figure 5-5. I²C Mode Timing

5.16 FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|-------------------------|-----------------------|-----|-----|--------|
| t _{WRITE} | Word or byte write time | | | 125 | ns |
| | Read/write endurance | 10 ¹⁵ | | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | 10 | | years |

5.17 JTAG

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | V _{DDB} | MIN | TYP | MAX | UNIT |
|------------------|------------------|-----|-----|-----|------|
| f _{TCK} | 1.5 V | 0 | | 4 | MHz |

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.18 RFPMM, Power Supply Switch

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|---|---|-----|-----|-----|------|
| V_{TH+} | Positive going switching threshold $V_{TH+} = V_{DDB} - V_{DDR}$ | | | 35 | 60 | mV |
| V_{TH-} | Negative going switching threshold $V_{TH-} = V_{DDB} - V_{DDR}$ | | -60 | -35 | | mV |
| V_{HYST} | Switching voltage hysteresis $V_{HYST} = V_{TH+} - V_{TH-}$ | | 30 | 70 | 110 | mV |
| $I_{BASVBAT}$ | V_{DDB} input leakage current | $V_{DDB} = 1.65$ V, Battery switch open | | | 20 | nA |
| V_{DROP} | $V_{DROP} = V_{DDB} - V_{DDSW}^{(1)}$ | | | | 50 | mV |

(1) Battery switch closed. Current = 400 μ A

5.19 RFPMM, Bandgap Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|----------------|------------------------------|-----|-----|-----|------|
| V_{REF} | Output voltage | $V_{DDSW} = 1.4$ V to 1.65 V | 892 | | 908 | mV |

5.20 RFPMM, Voltage Doubler

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|----------------|--|-----|------------------------------|-----|------|
| V_{DD2X} | Output voltage | $V_{DDSW} = 1.4$ V, $I_{DD2X} = 1$ μ A, cont = 0 | | $2 \times V_{DDSW} - 74$ mV | | mV |
| V_{DD2X} | Output voltage | $V_{DDSW} = 1.4$ V, $I_{DD2X} = 100$ μ A, cont = 1 | | $2 \times V_{DDSW} - 104$ mV | | mV |

5.21 RFPMM, Voltage Supervision

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V_{DDSW} | MIN | TYP | MAX | UNIT |
|---------------|--------------------|------------|-----|-------|-----|------|
| V_{DDBTH+} | Positive threshold | 1.5 V | | 1.45 | | V |
| V_{DDBTH-} | Negative threshold | 1.5 V | | 1.40 | | V |
| $V_{DDSWTH+}$ | Positive threshold | | | 1.40 | | V |
| $V_{DDSWTH-}$ | Negative threshold | | | 1.35 | | V |
| V_{DDDTH+} | Positive threshold | 1.5 V | | 1.00 | | V |
| V_{DDDTH-} | Negative threshold | 1.5 V | | 0.90 | | V |
| $V_{DD2XTH+}$ | Positive threshold | 1.5 V | | 2.70 | | V |
| $V_{DD2XTH-}$ | Negative threshold | 1.5 V | | 2.475 | | V |

5.22 SD14, Performance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|-----------------------|--|--|-------|-----|-----------|-------------------------|
| f_M | Modulator clock frequency | Internal LF oscillator as clock source for SD14 module | | 2 | | kHz |
| RES | Resolution | | 8 | | 14 | Bit |
| OSR | Oversampling ratio | | 40 | | 2048 | |
| B | Bandwidth of input signal | | | | 1 | Hz |
| V_I | Input voltage range | $V_I = V_{ADCx} - V_{SVSS}$ | 0 | | V_{REF} | mV |
| V_{offset} | Offset error | Complete signal chain | -0.75 | | 0.75 | % of FSR ⁽¹⁾ |
| V_{GErr} | Gain error ⁽²⁾ | complete signal chain | -2% | | 2% | |
| $\Delta E_G/\Delta T$ | Gain error temperature coefficient. ⁽³⁾ | complete signal chain | | | 100 | ppm/K |
| $E_{Unadjusted}$ | Total unadjusted error | | -2 | | 2 | % of FSR ⁽¹⁾ |
| t_{Start} | Startup time | | | 20 | | CLK cycles |

(1) FSR = Full Scale Range (SD14 pre-amplifier Gain PGA gain - SD14 gain =1) .

(2) The gain error E_G specifies the deviation of the actual gain G_{act} from the nominal gain G_{nom} : $E_G = (G_{act} - G_{nom})/G_{nom}$. It covers process, temperature and supply voltage variations.

(3) Not production tested.

5.23 SVSS Generator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|--|-----|-----|------|------|
| V_{SVSS} | Output voltage | $I_{SVSS} = -5\mu A \dots 0\mu A$ | 80 | 125 | 165 | mV |
| $t_{Settling}$ | Settling time after switching SVSS on (95% of final voltage) | Switch from VIRTGND = 1 to VIRTGND = 0 | | 400 | 1000 | ms |

5.24 Thermistor Bias Generator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|----------------|------------------------|-----|-----|-----|---------|
| $I_{OUT,TH}$ | Output current | $V_{OUT} = 0$ to 0.7 V | 2.0 | 2.4 | 3.0 | μ A |

5.25 Temperature Sensor

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|-----------------|-----|------|-----|-------|
| t_c | Temperature coefficient | | | 35.7 | | LSB/K |

5.26 RF13M, Power Supply and Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---------------------------|-----------------------|------|-----|------|------|
| V_{DDH} | Antenna rectified voltage | $I_{DDH} = 100 \mu$ A | 1.8 | 2 | 3.6 | V |
| C_{IN} | Input capacitance | 2 V RMS | 31.5 | 35 | 38.5 | pF |

5.27 RF13M, ISO/IEC 15693 ASK Demodulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-----|-----|------|---------|
| DR_{100} | Input signal data rate 100% downlink modulation, 100% ASK, ISO/IEC 15693 | | 6 | | 26 | kbps |
| m_{100} | Modulation depth 100%, test as defined in ISO10373 | | 90% | | 100% | |
| m_{10} | Modulation depth 10%, test as defined in ISO10373 | | 7% | | 30% | |
| $ t_{PLH} - t_{PHL} $ | Delta propagation delay of RXD_10 to V_{IN} | | 0 | | 2.35 | μ s |
| t_{PLH}, t_{PHL} | Propagation delay of RXD_10 to V_{IN} | | 0 | | 7.07 | μ s |
| t_{pd100} | Propagation delay of RXD_100 | | | | 7.07 | μ s |
| t_{D100} | Minimum pulse duration of RxD_100 | | 5 | | | μ s |

5.28 RF13M, ISO/IEC 15693 Compliant Load Modulator

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|---|-----------------|-----|-----|-----|------|
| f_{PICC} | Uplink subcarrier modulation frequency | | 0.2 | | 1 | MHz |
| V_{A_MOD} | Modulated antenna voltage, $V_{A_unmod} = 2,3$ V | | 0.5 | | | V |
| V_{SUB15} | Uplink modulation subcarrier level, ISO/IEC 15693 | | 10 | | | mV |

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-Bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

6.2 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data.

6.3 Operating Modes

The device has one active mode and three software selectable low-power modes of operation. An interrupt event can wake up the device from any of the three low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

NOTE

The software-selected low-power mode might not be reached if at least one module still requests a clock on MCLK, SMCLK, or ACLK. The CPU, however, remains off until an interrupt occurs.

The following operating modes can be configured by software:

- Active mode AM
 - CPU is enabled
 - All clocks are active.
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - MCLK is disabled
 - SMCLK is active
 - ACLK is active
 - HFOSC is off, if not selected for SMCLK or ACLK
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK is disabled
 - SMCLK is disabled
 - ACLK is active
 - HFOSC is off, if not selected for ACLK
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - MCLK is disabled
 - SMCLK is disabled
 - ACLK is disabled
 - HFOSC is off, LFOSC is on

LPM1 is identical to LPM0, and LPM2 is identical to LPM3, because the SCG0 bit has no influence on HFOSC.

6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FFE0h. Address Range 0FFDFh to 0FFD0h is reserved for bootcode signatures. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-1. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|---|---|------------------|--------------|-------------|
| System Reset Power-Up External Reset Watchdog | WDTIFG ⁽¹⁾ | Reset | FFFEh | 15, highest |
| System NMI Vacant memory access | SVMIFG, VMAIFG ⁽¹⁾ | (Non)maskable | 0FFFCCh | 14 |
| User NMI NMI | NMIIFG ⁽¹⁾⁽²⁾ | (Non)maskable | 0FFFAh | 13 |
| TimerA0_A3 | TA0CCR0 CCIFG0 ⁽³⁾ | Maskable | 0FFF8h | 12 |
| TimerA0_A3 | TA0CCR1 CCIFG1 TA0CCR2 CCIFG2 TA0CTL TAIFGTA0IV ⁽¹⁾⁽³⁾ | Maskable | 0FFF6h | 11 |
| Watchdog, Interval Timer Mode | WDTIFG | Maskable | 0FFF4h | 10 |
| RF13M Module | RF13MRXIFG, RF13MTXIFG, RF13MRXWMIFG, RF13MTXWMIFG, RF13MSLIFG, RF13MOUFLIFG, RF13MRXEIFG, RF13MIV _x ⁽¹⁾⁽³⁾ | Maskable | 0FFF2h | 9 |
| eUSCIB | (SPI mode) UCB0RXIFG, UCB0TXIFG (I ² C mode) UCB0ALIFG, UCB0NACKIFG, UCB0STTIFG, UCB0STPIFG, UCB0RXIFG3, UCB0TXIFG3, UCB0RXIFG2, UCB0TXIFG2, UCB0RXIFG1, UCB0TXIFG1, UCB0RXIFG0, UCB0TXIFG0, UCB0CNTIFG, UCB0CLTOIFG, UCB0BIT9IFG (SD14IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFF0h | 8 |
| Sigma Delta ADC | SD14OVIFG, SD14IFG ⁽¹⁾⁽³⁾ | Maskable | 0FFEEh | 7 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ⁽¹⁾⁽³⁾ | Maskable | 0FFECCh | 6 |
| RFPMM | RFPMMIFGV2X, RFPMMIFGVH, RFPMMIFGVR, RFPMMIFGVB, RFPMMIFGVF, RFPMMIV | Maskable | 0FFEAh | 5 |
| Reserved | Reserved ⁽⁴⁾ | | 0FFE8h | 4 |
| | | | : | : |
| | | | 0FFDCh | 0 |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(3) Interrupt flags are located in the module.

(4) Reserved interrupt vectors at these addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Table 6-1. Interrupt Sources, Flags, and Vectors (continued)

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------|--------------------|------------------|--------------|----------|
| Signatures | CRC Value | | 0FFDAh | |
| | CRC Length | | 0FFD8h | |
| | Loader Signature 1 | | 0FFD6h | |
| | Loader Signature 0 | | 0FFD4h | |
| | JTAG Signature 1 | | 0FFD2h | |
| | JTAG Signature 0 | | 0FFD0h | |

6.5 Memory

Table 6-2 shows the memory organization of the devices.

Table 6-2. Memory Map RF430FRL152H, RF430FRL153H, RF430FRL154H

| | TYPE | RF430FRL152H RF430FRL153H RF430FRL154H Normal Mode | RF430FRL152H RF430FRL153H RF430FRL154H ROM Development Mode |
|---|--------------------------|---|--|
| Memory (FRAM) Main: interrupt vector | Total Size FRAM | 2048 B = 2 KB 0FFFFh-0FFE0h | |
| Main: Code Memory | Bank A ⁽¹⁾⁽²⁾ | 512 B 0FFFFh-0FE00h | |
| | Bank B ⁽¹⁾ | 512 B 0FDFFh-0FC00h | |
| | Bank C ⁽¹⁾ | 512 B 0FBFFh-0FA00h | |
| | Bank D | 448 B 0F9FFh-0F840h | |
| Boot Data (TLV) | Size FRAM | 64 B 01A3Fh-01A00h | 64 B 01A3Fh-01A00h |
| Application ROM | Size ROM | 7168 B = 7 KB 05FFFh-04400h | 3584 B = 3.5 KB 051FFh-04400h |
| ROM Development Memory | Size SRAM | - - | 3584 B = 3.5 KB 02BFFh-01E00h |
| SRAM Memory | Size SRAM | 4096 B = 4 KB 02BFFh-01C00h | 512 B = 0.5 KB 01DFFh-01C00h |
| Peripherals | Size | 4096 B = 4 KB 00FFFh-00000h | 4096 B = 4 KB 00FFFh-00000h |

(1) Write protectable. See also [Table 6-3](#)

(2) Address range includes interrupt vector.

6.5.1 FRAM

The FRAM can be programmed through the JTAG port or in-system by the CPU, data are received through RF, SPI or I²C Sensor Interface.

Features of the FRAM include:

- Low-power ultra-fast-write non-volatile memory
- Byte and word access capability
- Automated wait state generation

The following address ranges can be write protected by setting the corresponding bit in the SYSCNF register, see the *RF430FRL15xH Family Technical Reference Manual* ([SLAU506](#)).

Table 6-3. Write Protectable FRAM Address Ranges

| BIT | Address Range |
|----------|------------------------|
| FRAMLCK2 | 512 B 0FFFFh-0FE00h |
| FRAMLCK1 | 512 B 0FDFFh-0FC00h |
| FRAMLCK0 | 512 B 0FBFFh-0FA00h |

6.5.2 SRAM

The SRAM memory is made up of 8 sectors. Each sector can be completely powered down to save leakage; however, all data is lost. Features of the SRAM memory include:

- SRAM memory has 8 sectors of 512 B each.
- Each sector 0 to 8 can be complete disabled; however, data retention is lost.
- Each sector 0 to 8 automatically enters low-power retention mode when possible.

6.5.3 Application ROM

The Application ROM consists of four parts. The RF Library provides ISO/IEC 15693 functions necessary for operating the 13.65 MHz front end. The Function library holds the device and memory function used by the boot code and RF library. These functions are user accessible. The ROM contains the predefined application FW. The boot code checks the password and releases control to the application or enables JTAG on password match, enters LPM4 and waits for debug session, see the *RF430FRL15xH Firmware User's Guide* ([SLAU603](#)).

6.6 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be managed using all instructions. For complete module descriptions, see the *RF430FRL15xH Family Technical Reference Manual* ([SLAU506](#)).

6.6.1 Digital I/O, (P1.x)

There is one I/O port implemented, P1, with eight I/O lines RF430FRL15xH.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown resistor on all ports.
- Edge-selectable interrupt input capability for all ports on P1.
- Read and write access to port-control registers is supported by all instructions.

6.6.2 Versatile I/O Port P1

The versatile I/O ports P1 feature device dependent reset values. The reset values for the RF430FRL15xH devices are shown in [Table 6-4](#).

Table 6-4. Versatile Port Reset Values

| PORT NUMBER | PxOUT | PxDIR | PxREN | PxSEL0 | PxSEL1 | RESET | PORTS ON | COMMENT |
|-------------|-------|-------|-------|--------|--------|-------|----------|------------------------|
| P1.0 | 0 | 0 | 0 | 0 | 0 | PUC | yes | P1.0, input |
| P1.1 | 0 | 0 | 0 | 0 | 0 | PUC | yes | P1.1, input |
| P1.2 | 0 | 0 | 0 | 0 | 0 | PUC | yes | P1.2, input |
| P1.3 | 0 | 0 | 0 | 0 | 0 | PUC | yes | P1.3, input |
| P1.4 | 1 | 0 | 1 | 1 | 1 | PUC | yes | JTAG TCK, P1.4, input |
| P1.5 | 1 | 0 | 1 | 1 | 1 | PUC | yes | JTAG TDI, P1.5, input |
| P1.6 | 0 | 0 | 0 | 1 | 1 | PUC | yes | JTAG TDO, P1.6, output |
| P1.7 | 1 | 0 | 1 | 1 | 1 | PUC | yes | JTAG TMS, P1.7, input |

6.6.3 Oscillator and System Clock

The clock system in the RF430FRL15xH devices is supported by the Compact Clock System (CCS) module that includes support for an internal trimmable 256-kHz current-controlled low-frequency oscillator (LFOSC) and an internal 4-MHz current-controlled high-frequency oscillator (HFOSC).

The CCS module is designed to meet the requirements of both low system cost and low power consumption. The CCS provides a fast turn-on of the oscillators in less than 1 ms. The CCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from the 256-kHz internal LFOSC.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.

6.6.4 Compact System Module (C-SYS_A)

The Compact SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, as well as, configuration management. It also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application.

Table 6-5. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | INTERRUPT VECTOR | WORD ADDRESS | OFFSET | PRIORITY |
|---------------------------|-----------------------------|--------------|---------|----------|
| SYSRSTIV, System Reset | No interrupt pending | 019Eh | 00h | |
| | Brownout (BOR) | | 02h | Highest |
| | SVMBOR (BOR) | | 04h | |
| | RST/NMI (BOR) | | 06h | |
| | DoBOR (BOR) | | 08h | |
| | Security violation (BOR) | | 0Ah | |
| | DoPOR (POR) | | 0Ch | |
| | WDT time-out (PUC) | | 0Eh | |
| | WDT key violation (PUC) | | 10h | |
| | CCS key violation | | 12h | |
| | PMM key violation | | 14h | |
| | Peripheral area fetch (PUC) | | 16h | |
| | Reserved | | 18h-3Eh | Lowest |
| SYSSNIV, System NMI | No interrupt pending | 019Ch | 00h | |
| | SVMIFG | | 02h | Highest |
| | VMAIFG | | 04h | |
| | JMBINIFG | | 06h | |
| | JMBOUTIFG | | 08h | |
| | Reserved | | 0Ah-3Eh | Lowest |
| SYSUNIV, User NMI | No interrupt pending | 019Ah | 00h | |
| | NMIFG | | 02h | Highest |
| | OFIFG | | 04h | |
| | BERR | | 06h | |
| | Reserved | | 08h-3Eh | Lowest |
| SYSBERRIV, Bus Error | No interrupt pending | 0198h | 00h | |
| | Reserved | | 02h-3Eh | Lowest |

6.6.5 Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.6.6 Reset, NMI, SVMOUT System

The reset system of the RF430FRL15xH devices features the function reset input, reset output, and NMI input.

6.6.7 Timer_A (Timer0_A3)

Timer_A is a 16-bit timer/counter with three capture/compare registers. Timer_A can support multiple capture/compares, PWM outputs, and interval timing. Timer_A also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-6. Timer0_A3 Signal Connections

| INPUT PIN NUMBER | DEVICE INPUT SIGNAL | MODUL INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL | OUTPUT PIN NUMBER |
|------------------|---------------------|--------------------|--------------|----------------------|----------------------|-------------------|
| 8 – P1.3 | TA0CLK | TACLK | Timer | NA | NA | |
| | ACLK (internal) | ACLK | | | | |
| | SMCLK (internal) | SMCLK | | | | |
| | TA0CLK | \overline{TACLK} | | | | |
| 12 – P1.0 | TA0.0 | CCI0A | CCR0 | TA0 | TA0.0 | 9 – P1.2 |
| 11 – P1.1 | TA0.0 | CCI0B | | | | 20 – P1.6 |
| | V _{SS} | GND | | | | 19 – P1.7 |
| | V _{DDB} | V _{CC} | | | | |
| 22 – P1.4 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 | 12 – P1.0 |
| 21 – P1.5 | TA0.1 | CCI1B | | | | 22 – P1.4 |
| | V _{SS} | GND | | | | 19 – P1.7 |
| | V _{DDB} | V _{CC} | | | | |
| 20 – P1.6 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 | 11 – P1.1 |
| 19 – P1.7 | TA0.2 | CCI2B | | | | 8 – P1.3 |
| | V _{SS} | GND | | | | 21 – P1.5 |
| | V _{DDB} | V _{CC} | | | | 20 – P1.6 |

6.6.8 Enhanced Universal Serial Communication Interface (eUSCI_B0)

The eUSCI_B0 module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 pin or 4 pin) and I²C.

The eUSCI_B0 module provides support for SPI (3 pin or 4 pin) or I²C.

6.6.9 ISO/IEC 15693 Analog Front End (RF13M)

The ISO/IEC 15693 module supports contact-less communication over the analog front end according to ISO/IEC 15693 with data rates up to 26.48 kbps for receive and 26.48 kbps for transmit. It includes decode of receive data and encode of transmit data, both synchronous with the AFE carrier clock.

6.6.10 ISO/IEC 15693 Decoder/Encoder (RF13M)

The module interfaces directly to the analog front end to ensure correct timing for transmit and receive of data derived from the 13.56-MHz carrier frequency.

6.6.11 CRC16 Module (CRC16)

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data

checking purposes. The CRC16 module is compliant with ISO/IEC 13239, it is 16 bits long, polynomial is: $x^{16} + x^{12} + x^5 + 1$, direction is backward, and preset is 0xFFFF. For more information see ISO/IEC 13239.

6.6.12 14-Bit Sigma-Delta ADC (SD14)

A sigma-delta modulator is provided for high resolution analog-to-digital conversion of quasi-dc voltages:

- First-order integrator, 1-bit comparator, 1-bit DAC
- Sampling frequency of up to 2 kHz
- Fully differential

6.6.13 Programmable Gain Amplifier (SD14)

The PGA features a very high-impedance input and a programmable gain combined with full offset compensation, very low offset drift, and low noise.

6.6.14 Peripheral Register Map

Table 6-7. Peripheral Register Map

| MODULE NAME | REGISTER DESCRIPTION | REGISTER | BASE ADDRESS | OFFSET |
|-------------------------|---|-------------|--------------|--------|
| RF13M | RF13M RX/TX High/Low Watermark Configuration Register | RF13MWMCFG | 0800h | 0Eh |
| | RF13M RX/TX FIFO Fill Level register | RF13MFIFOFL | | 0Ch |
| | RF13M CRC accumulator Register | RF13MCRC | | 0Ah |
| | RF13M Transmit Data FIFO Register | RF13MTXF | | 08h |
| | RF13M Receive Data FIFO Register | RF13MRXF | | 06h |
| | RF13M Interrupt Vector Register | RF13MIV | | 04h |
| | RF13M Interrupt Register | RF13MINT | | 02h |
| | RF13M Control Register | RF13MCTL | | 00h |
| SD14 | SD14 Interrupt Vector Register | SD14IV | 0700h | 0Ch |
| | SD14 Intermediate Conversion Result Register | SD14MEM3 | | 0Ah |
| | SD14 Intermediate Conversion Result Register | SD14MEM2 | | 08h |
| | SD14 Intermediate Conversion Result Register | SD14MEM1 | | 06h |
| | SD14 Conversion Result | SD14MEM0 | | 04h |
| | SD14 Control Register 1 | SD14CTL1 | | 02h |
| | SD14 Control Register 0 | SD14CTL0 | | 00h |
| eUSCI_B0 | Interrupt Vector Word Register | UCB0IV | 0640h | 2Eh |
| | Interrupt Flags Register | UCB0IFG | | 2Ch |
| | Interrupt Enable Register | UCB0IE | | 2Ah |
| | I2C Slave Address Register | UCB0I2CSA | | 20h |
| | Address Mask Register | UCB0ADDMASK | | 1Eh |
| | Received Address Register | UCB0ADDRX | | 1Ch |
| | I2C Own Address 3 Register | UCB0I2COA3 | | 1Ah |
| | I2C Own Address 2 Register | UCB0I2COA2 | | 18h |
| | I2C Own Address 1 Register | UCB0I2COA1 | | 16h |
| | I2C Own Address 0 Register | UCB0I2COA0 | | 14h |
| | Transmit Buffer Register | UCB0TXBUF | | 0Eh |
| | Receive Buffer Register | UCB0RXBUF | | 0Ch |
| | Byte Counter Threshold Register | UCB0TBCNT | | 0Ah |
| | Status Word Register | UCB0STATW | | 08h |
| | Bit Rate 1 Register | UCB0BR1 | | 07h |
| | Bit Rate 0 Register | UCB0BR0 | | 06h |
| | Control Word 1 Register | UCB0CTLW1 | | 02h |
| Control Word 0 Register | UCB0CTLW0 | 00h | | |

Table 6-7. Peripheral Register Map (continued)

| MODULE NAME | REGISTER DESCRIPTION | REGISTER | BASE ADDRESS | OFFSET |
|--|---|---------------------------------|--------------|----------|
| Timer0_A3 | Timer0_A Interrupt Vector Register | TA0IV | 0340h | 2Eh |
| | Capture/Compare Register 2 | TA0CCR2 | | 16h |
| | Capture/Compare Register 1 | TA0CCR1 | | 14h |
| | Capture/Compare Register 0 | TA0CCR0 | | 12h |
| | Timer0_A Counter Register | TA0R | | 10h |
| | Capture/Compare Control 2 Register | TA0CCTL2 | | 06h |
| | Capture/Compare Control 1 Register | TA0CCTL1 | | 04h |
| | Capture/Compare Control 0 Register | TA0CCTL0 | | 02h |
| | Timer0_A Control Register | TA0CTL | | 00h |
| Port P1 | Port P1 Interrupt Flag Register | P1IFG | 0200h | 1Ch |
| | Port P1 Interrupt Enable Register | P1IE | | 1Ah |
| | Port P1 Interrupt Edge Select Register | P1IES | | 18h |
| | Port P1 Interrupt Vector Word Register | P1IV | | 0Eh |
| | Port P1 Selection 1 Register | P1SEL1 | | 0Ch |
| | Port P1 Selection 0 Register | P1SEL0 | | 0Ah |
| | Port P1 Pullup/Pulldown Enable Register | P1REN | | 06h |
| | Port P1 Direction Register | P1DIR | | 04h |
| | Port P1 Outout Register | P1OUT | | 02h |
| | Port P1 Input Register | P1IN | | 00h |
| | CSYS_A | Reset Vector Generator Register | | SYSRSTIV |
| System NMI Vector Generator Register | | SYSSNIV | 1Ch | |
| User NMI Vector Generator Register | | SYSUNIV | 1Ah | |
| Bus Error Vector Generator Register | | SYSBERRIV | 18h | |
| System Configuration Actuator 0 Register | | SYSCA0 | 14h | |
| System Configuration Register | | SYSCNF | 10h | |
| JTAG Mailbox Output Register 1 | | SYSJMBO1 | 0Eh | |
| JTAG Mailbox Output Register 0 | | SYSJMBO0 | 0Ch | |
| JTAG Mailbox Input Register 1 | | SYSJMBI1 | 0Ah | |
| JTAG Mailbox Input Register 0 | | SYSJMBI0 | 08h | |
| JTAG Mailbox Control Register | | SYSJMBC | 06h | |
| System Control Register | | SYSCTL | 00h | |
| CCS | CCS Control 8 Register | CCSCTL8 | 0160h | 10h |
| | CCS Control 7 Register | CCSCTL7 | | 0Eh |
| | CCS Control 6 Register | CCSCTL6 | | 0Ch |
| | CCS Control 5 Register | CCSCTL5 | | 0Ah |
| | CCS Control 4 Register | CCSCTL4 | | 08h |
| | CCS Control 1 Register | CCSCTL1 | | 02h |
| | CCS Control 0 Register | CCSCTL0 | | 00h |
| WDT_A, CRC | Watchdog Timer Control Register | WDTCTL | 0150h | 0Ch |
| | CRC Result Reverse Register | CRCRESR | | 06h |
| | CRC Initialization and Result Register | CRCINIRES | | 04h |
| | CRC Data In Reverse Byte Register | CRCDIRB | | 02h |
| | CRC Data In Register | CRCDI | | 00h |
| FRAM Control | General Control 1 Register | GCCTL1 | 0140h | 06h |
| | General Control 0 Register | GCCTL0 | | 04h |
| | FRAM Control 0 Register | FRCTL0 | | 00h |

Table 6-7. Peripheral Register Map (continued)

| MODULE NAME | REGISTER DESCRIPTION | REGISTER | BASE ADDRESS | OFFSET |
|-------------------|---------------------------------|-----------|--------------|--------|
| RFPMM | RFPMM Interrupt Vector Register | RFPMMIV | 0120h | 08h |
| | RFPMM Interrupt Flag Register | RFPMMIFG | | 06h |
| | RFPMM Interrupt Enable Register | RFPMMIE | | 04h |
| | RFPMM Control Register 1 | RFPMMCTL1 | | 02h |
| | RFPMM Control Register 0 | RFPMMCTL0 | | 00h |
| Special Functions | SFR Reset Pin Control Register | SFRRPCR | 0100h | 04h |
| | SFR Interrupt Flag Register | SFRIFG1 | | 02h |
| | SFR Interrupt Enable Register | SFRIE1 | | 00h |

6.7 Port Schematics

6.7.1 Port P1.0 Input/Output

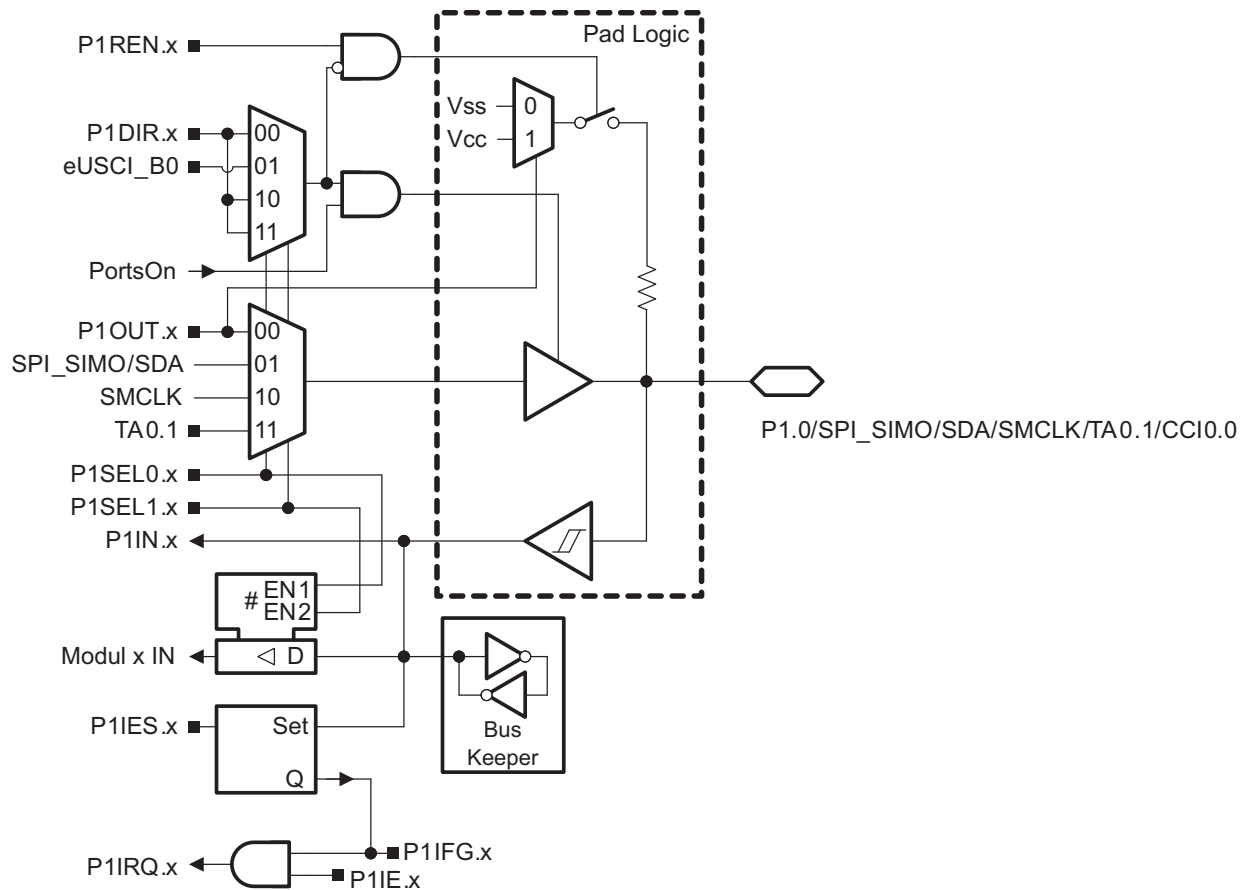


Table 6-8. Port P1.0 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|--------------------------------------|---|-----------------------------|--|----------|----------|-----------------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | RSELx/ ASELx |
| P1.0/SPI_SIMO/SDA/SMCLK/TA0.1/CCI0.0 | 0 | P1.0 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | SPI_SIMO/SDA ⁽²⁾ | 1 | 0 | 1 | 0 |
| | | SMCLK | 1 | 1 | 0 | 0 |
| | | TA0.1 | 1 | 1 | 1 | 0 |
| | | Timer A0, CCI0A | 0 | ≠0 | ≠0 | X |

(1) X = Don't care

(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.2 Port P1.1 Input/Output

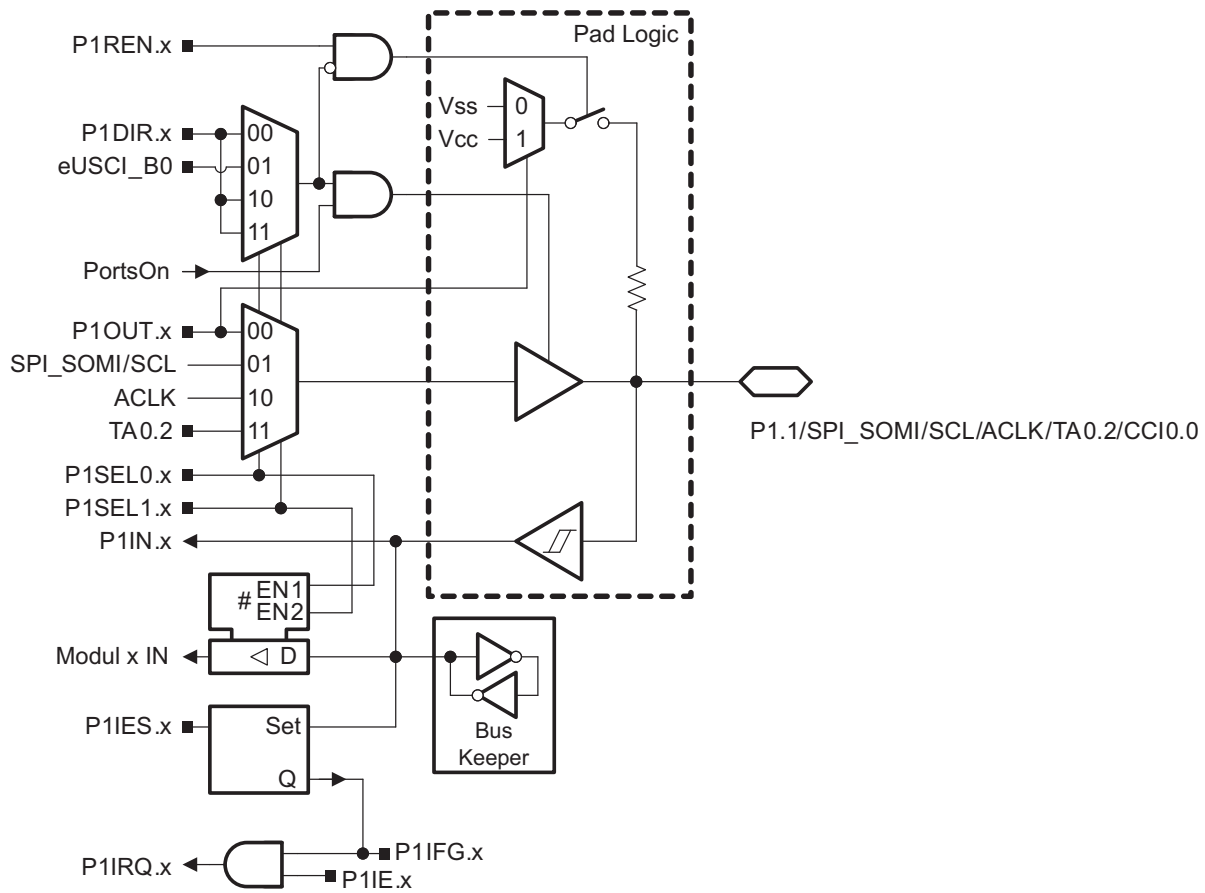


Table 6-9. Port P1.1 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-------------------------------------|---|-----------------------------|--|----------|----------|--------------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | RSELx/ASE Lx |
| P1.1/SPI_SOMI/SCL/ACLK/TA0.2/CCI0.0 | 1 | P1.1 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | SPI_SOMI/SCL ⁽²⁾ | 1 | 0 | 1 | 0 |
| | | ACLK | 1 | 1 | 0 | 0 |
| | | TA0.2 | 1 | 1 | 1 | 0 |
| | | Timer A1, CCI0B | 0 | ≠0 | ≠0 | X |

(1) X = Don't care

(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.3 Port P1.2 Input/Output

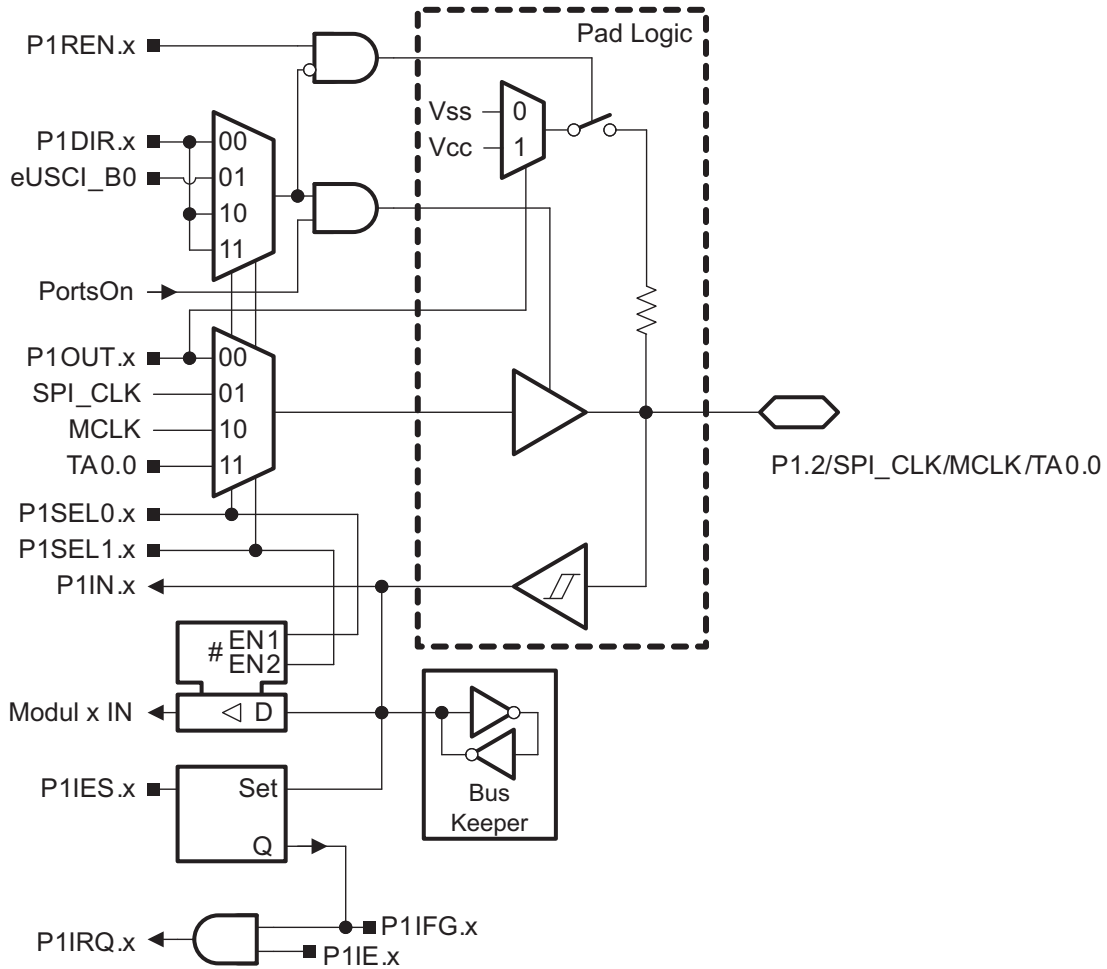


Table 6-10. Port P1 (P1.2) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-------------------------|---|------------------------|--|----------|----------|-------------------------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | RSELx/ASEL _x |
| P1.2/SPI_CLK/MCLK/TA0.0 | 2 | P1.2 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | SPI_CLK ⁽²⁾ | 1 | 0 | 1 | 0 |
| | | MCLK | 1 | 1 | 0 | 0 |
| | | TA0.0 | 1 | 1 | 1 | 0 |

(1) X = Don't care

(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.4 Port P1.3 Input/Output

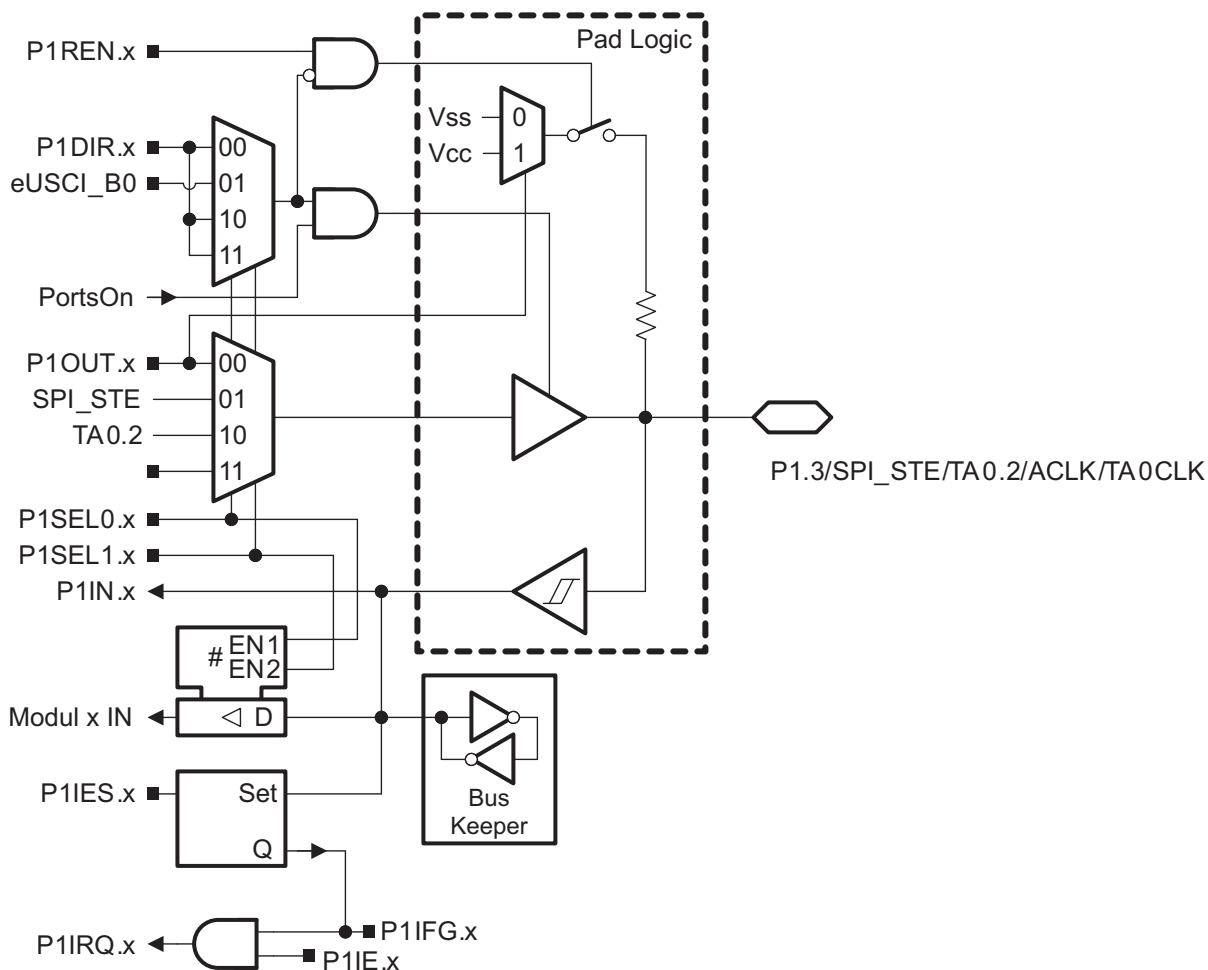


Table 6-11. Port P1 (P1.3) Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|--------------------------------|---|------------------------|--|----------|----------|--------------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | RSELx/ASE Lx |
| P1.3/SPI_STE/TA0.2/ACLK/TA0CLK | 3 | P1.3 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | SPI_STE ⁽²⁾ | 1 | 0 | 1 | 0 |
| | | TA0.2 | 1 | 1 | 0 | 0 |
| | | ACLK | 1 | 1 | 1 | 0 |
| | | TA0CLK | X | ≠0 | ≠0 | X |

(1) X = Don't care

(2) Module controls direction of port, depending on whether RF430 device is master or slave.

6.7.5 Port P1.4 Input/Output

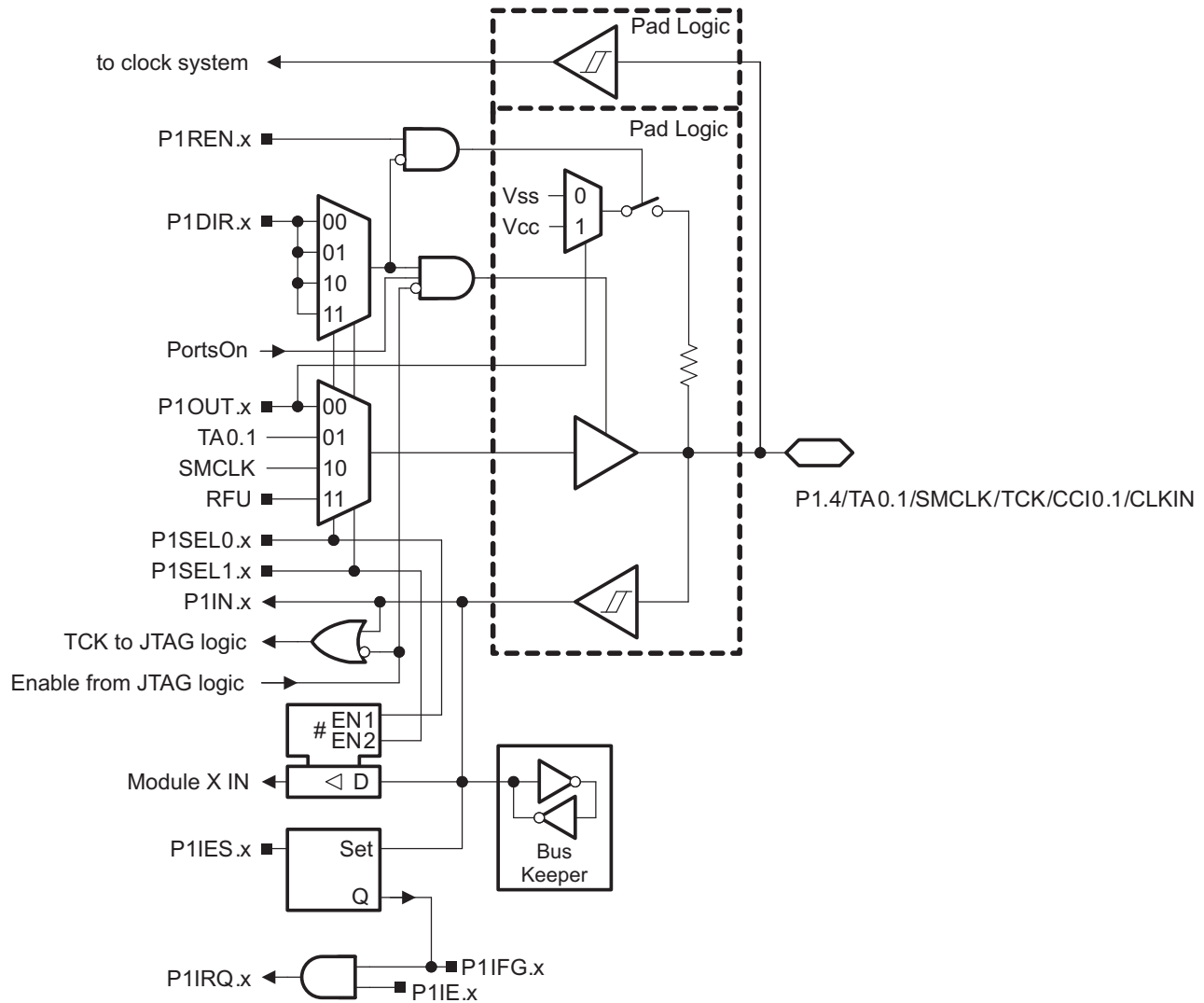


Table 6-12. Port P1.4 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------------------|---|-------------------------------|--|----------|----------|-----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | JTAG Mode |
| TCK/P1.4/TA0.1/SMCLK/CCI0.1 | 4 | P1.4 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | Timer_A0.1 | 1 | 0 | 1 | 0 |
| | | SMCLK | 1 | 1 | 0 | 0 |
| | | Reserved | 1 | 1 | 1 | 0 |
| | | Timer_A0.CCI1A | 0 | ≠0 | ≠0 | 0 |
| | | JTAG-TCK ⁽²⁾⁽³⁾⁽⁴⁾ | X | X | X | 1 |
| | | CLKIN from bypass | X | X | X | 0 |

- (1) X = Don't care
- (2) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.
- (3) JTAG overrides digital output control when configured as explicit JTAG terminals.
- (4) JTAG function with enabled pullup resistors is default after power up.

6.7.6 Port P1.5 Input/Output

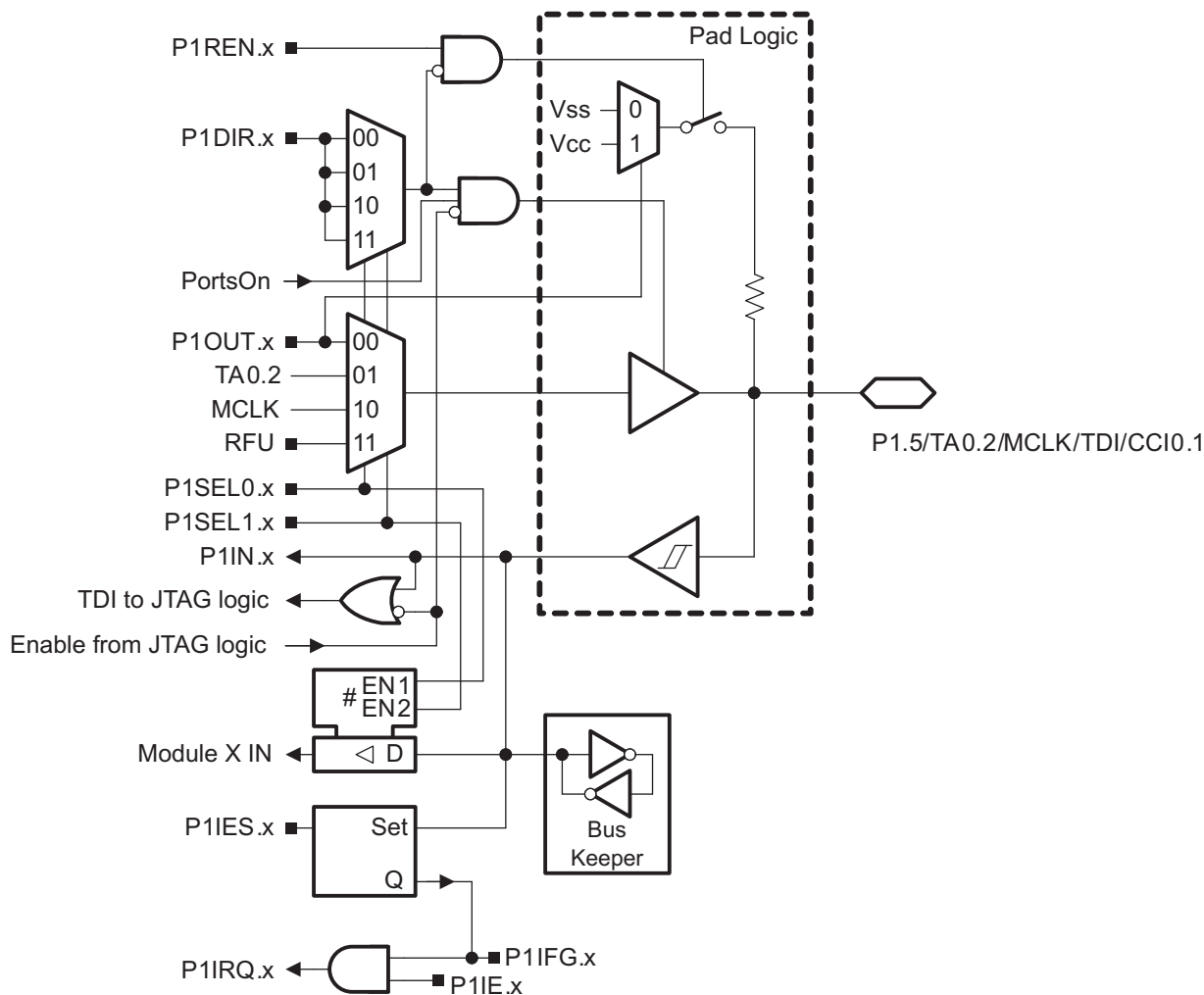


Table 6-13. Port P1.5 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-------------------------------|---|----------------|--|----------|----------|-----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | JTAG Mode |
| TDI/P1.5/TA0.2/MCLK/CCI0.1 | 5 | P1.5 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | Timer_A0.2 | 1 | 0 | 1 | 0 |
| | | MCLK | 1 | 1 | 0 | 0 |
| | | | 1 | 1 | 1 | 0 |
| | | Timer_A0 CCI1B | 0 | ≠0 | ≠0 | 0 |
| JTAG-TDI ⁽²⁾⁽³⁾⁽⁴⁾ | | | X | X | X | 1 |

- (1) X = Don't care
- (2) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.
- (3) JTAG overrides digital output control when configured as explicit JTAG terminals.
- (4) JTAG function with enabled pullup resistors is default after power up.

6.7.7 Port P1.6 Input/Output

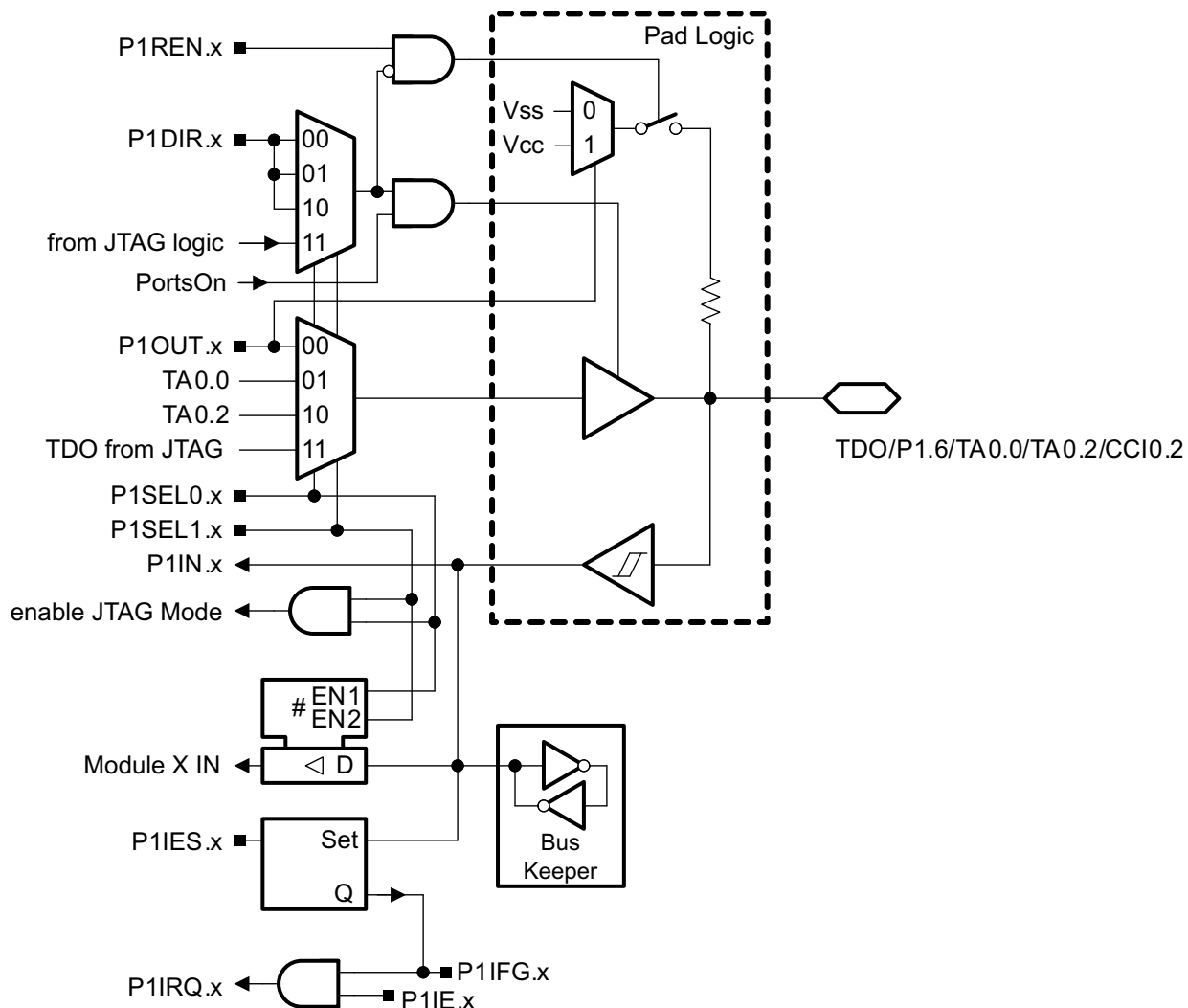


Table 6-14. Port P1.6 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|-----------------------------|---|----------------------------|-------------------------|----------|----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| TDO/P1.6/TA0.0/TA0.2/CCI0.2 | 6 | P1.6 (I/O) | I:0; O:1 | 0 | 0 |
| | | Timer_A0.0 | 1 | 0 | 1 |
| | | Timer_A0.2 | 1 | 1 | 0 |
| | | JTAG-TDO ⁽¹⁾⁽²⁾ | 1 | 1 | 1 |
| | | Timer_A0 CCI2A | 0 | ≠0 | ≠0 |

(1) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.

(2) JTAG overrides digital output control when configured as explicit JTAG terminals.

6.7.8 Port P1.7 Input/Output

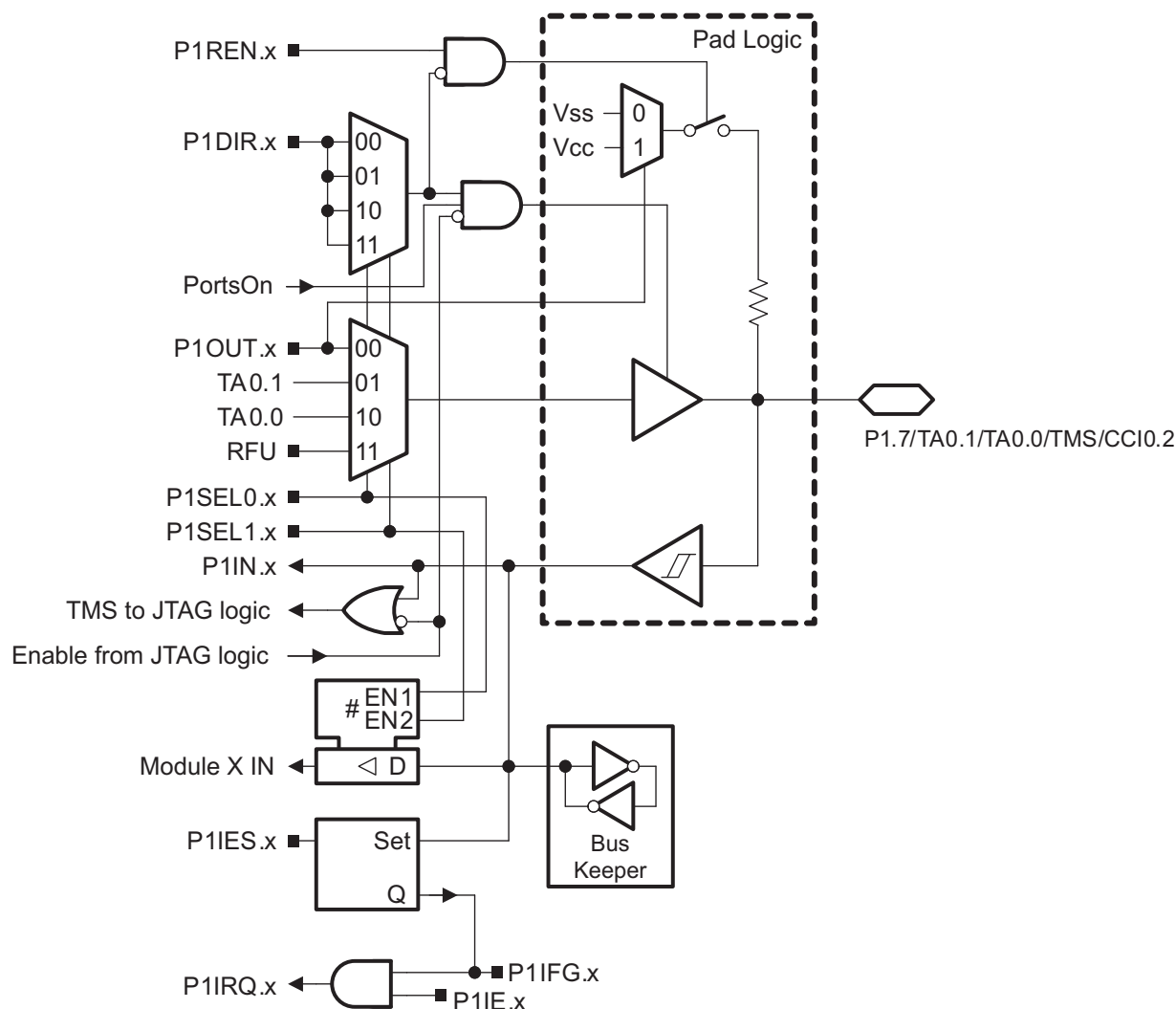


Table 6-15. Port P1.7 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-----------------------------|---|-------------------------------|--|----------|----------|-----------|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x | JTAG Mode |
| TMS/P1.7/TA0.1/TA0.0/CCI0.2 | 7 | P1.7 (I/O) | I:0; O:1 | 0 | 0 | 0 |
| | | Timer_A0.1 | 1 | 0 | 1 | 0 |
| | | Timer_A0.0 | 1 | 1 | 0 | 0 |
| | | Reserved | 1 | 1 | 1 | 0 |
| | | Timer_A0.CCI2B | 0 | ≠0 | ≠0 | 0 |
| | | JTAG-TMS ⁽²⁾⁽³⁾⁽⁴⁾ | X | X | X | 1 |

- (1) X = Don't care
- (2) JTAG signals TMS, TCK, and TDI read as 1 when not configured as explicit JTAG terminals.
- (3) JTAG overrides digital output control when configured as explicit JTAG terminals.
- (4) JTAG function with enabled pullup resistors is default after power up.

6.8 Device Descriptors (TLV)

Table 6-16 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

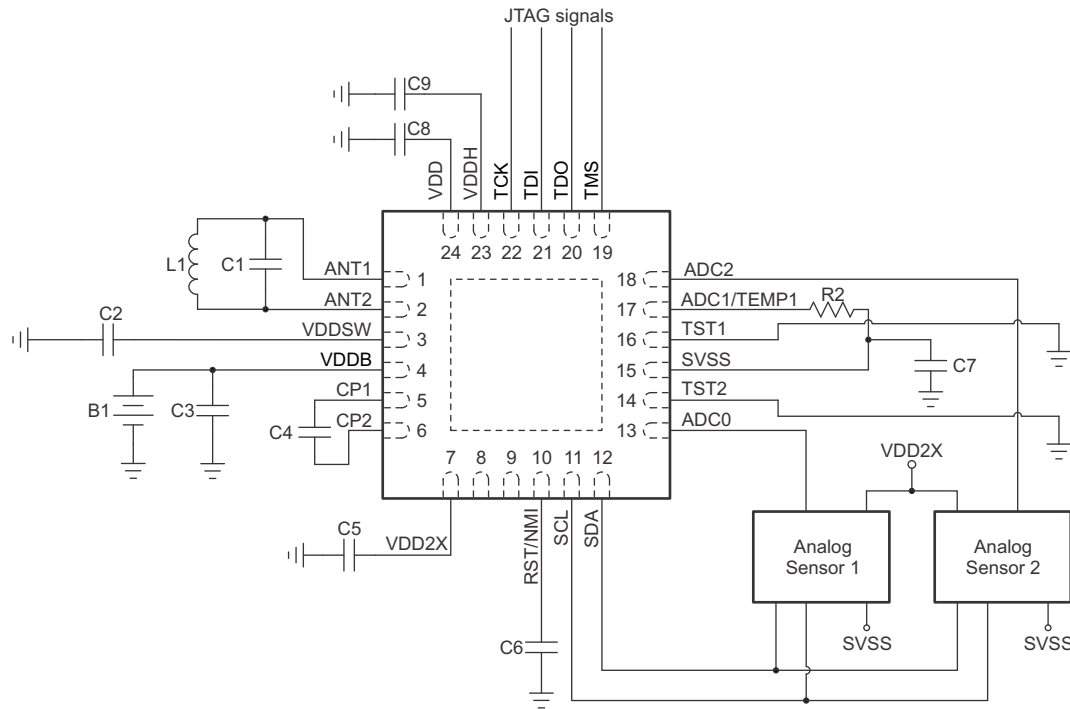
Table 6-16. RF430FRL15xH Boot Data and Device Descriptor Table

| | Description | Address | Size bytes | FRL152H | FRL153H | FRL154H |
|--------------------|-----------------------|----------------|------------|-----------|-----------|-----------|
| Info Block | Boot Data Length | 01A00h | 1 | 03h | 03h | 03h |
| | CRC length | 01A01h | 1 | 03h | 03h | 03h |
| | Boot Data CRC value | 01A02h | 2 | per unit | per unit | per unit |
| | Device ID | 01A04h | 1 | E7h | FBh | FCb |
| | Device ID | 01A05h | 1 | 81h | 81h | 81h |
| Die Record | Lot #0 | 01A06h | 1 | per unit | per unit | per unit |
| | Lot #1 | 01A07h | 1 | per unit | per unit | per unit |
| | UID0 | 01A08h | 1 | per unit | per unit | per unit |
| | UID1 | 01A09h | 1 | per unit | per unit | per unit |
| | UID2 | 01A0Ah | 1 | per unit | per unit | per unit |
| | UID3 | 01A0Bh | 1 | per unit | per unit | per unit |
| | UID4 | 01A0Ch | 1 | per unit | per unit | per unit |
| | UID5 | 01A0Dh | 1 | A2h / A3h | A2h / A3h | A2h / A3h |
| | Lot #2 | 01A0Eh | 1 | per unit | per unit | per unit |
| | Fab ID / Wafer Number | 01A0Fh | 1 | per unit | per unit | per unit |
| | Reserved | 01A10h | 2 | 0FFFFh | 0FFFFh | 0FFFFh |
| Reserved | 01A12h | 2 | 0FFFFh | 0FFFFh | 0FFFFh | |
| Calibration | Calibration Pointer | 01A14h | 2 | 01A14h | 01A14h | 01A14h |
| | Reserved | 01A16h | 2 | per unit | per unit | per unit |
| | Reserved | 01A18h | 2 | per unit | per unit | per unit |
| | Reserved | 01A1Ah | 2 | per unit | per unit | per unit |
| | Reserved | 01A1Ch | 2 | per unit | per unit | per unit |
| | Reserved | 01A1Eh | 2 | per unit | per unit | per unit |
| ECC | ECC of previous data | 01A3E - 01A20h | 32 | per unit | per unit | per unit |

Table 6-17. UID (Unique Identifier) Definition

| Description | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|-------------|---------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Lot ID 0 | 0x1A06 | LotNr[7] | LotNr[6] | LotNr[5] | LotNr[4] | LotNr[3] | LotNr[2] | LotNr[1] | LotNr[0] |
| Lot ID 1 | 0x1A07 | LotNr[15] | LotNr[14] | LotNr[13] | LotNr[12] | LotNr[11] | LotNr[10] | LotNr[9] | LotNr[8] |
| UID0 | 0x1A08 | TI[7] | TI[6] | TI[5] | TI[4] | TI[3] | TI[2] | TI[1] | TI[0] |
| UID1 | 0x1A09 | TI[15] | TI[14] | TI[13] | TI[12] | TI[11] | TI[10] | TI[9] | TI[8] |
| UID2 | 0x1A0A | TI[23] | TI[22] | TI[21] | TI[20] | TI[19] | TI[18] | TI[17] | TI[16] |
| UID3 | 0x1A0B | TI[31] | TI[30] | TI[29] | TI[28] | TI[27] | TI[26] | TI[25] | TI[24] |
| UID4 | 0x1A0C | TI[39] | TI[38] | TI[37] | TI[36] | TI[35] | TI[34] | TI[33] | TI[32] |
| UID5 | 0x1A0D | 1 | 0 | 1 | 0 | 0 | 0 | 1 | TI[40] |
| Lot ID 2 | 0x1A0E | LotNr[23] | LotNr[22] | LotNr[21] | LotNr[20] | LotNr[19] | LotNr[18] | LotNr[17] | LotNr[16] |
| FabID | 0x1A0F | Wafer[4] | Wafer[3] | Wafer[2] | Wafer[1] | Wafer[0] | FabNr[2] | FabNr[1] | FabNr[0] |

7 Applications, Implementation, and Layout



Two analog sensors connected through I²C, supplied by VDD2X (≈3 V)

Figure 7-1. Application Circuit

Table 7-1 lists the bill of materials for this application.

Table 7-1. Bill of Materials

| Name | Value | Description |
|------|----------------|---|
| L1 | 3 μ H | RF inductance (nominal) |
| C1 | 8.2 pF | RF tuning capacitor (nominal) |
| C2 | 2.2 μ F | Decoupling cap at VDDSW |
| C3 | 100 nF | Decoupling cap at VDDDB |
| C4 | 10 nF | Charge pump capacitor |
| C5 | 100 nF | Decoupling cap at VDD2X |
| C6 | 10 nF | Decoupling cap at RST |
| C7 | 1 μ F | Bypass capacitor between SVSS and V _{SS} |
| C8 | 100 nF | Decoupling cap at VDD |
| C9 | 100 nF | Decoupling cap at VDDH |
| B1 | 1.5 V | Battery |
| R2 | 100 k Ω | Reference resistor |

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

For an overview of the development tool and driver support for NFC transponders, visit the [Tools & Software for NFC / RFID](#) page.

8.1.2 Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all RF430 MCU devices and support tools. Each commercial family member has one of three prefixes: RF, P, or X (for example, RF430FRL152H). Texas Instruments recommends two of three possible prefix designators for its support tools: RF and X. These prefixes represent evolutionary stages of product development from engineering prototypes (with X for devices and tools) through fully qualified production devices and tools (with RF for devices tools).

Device development evolutionary flow:

X – Experimental device that is not necessarily representative of the final device's electrical specifications

P – Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

RF – Fully qualified production device

Support tool development evolutionary flow:

X – Development-support product that has not yet completed Texas Instruments internal qualification testing.

RF – Fully-qualified development-support product

X and P devices and X development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

RF devices and RF development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X and P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGE) and temperature range (for example, T). [Figure 8-1](#) provides a legend for reading the complete device name for any family member.

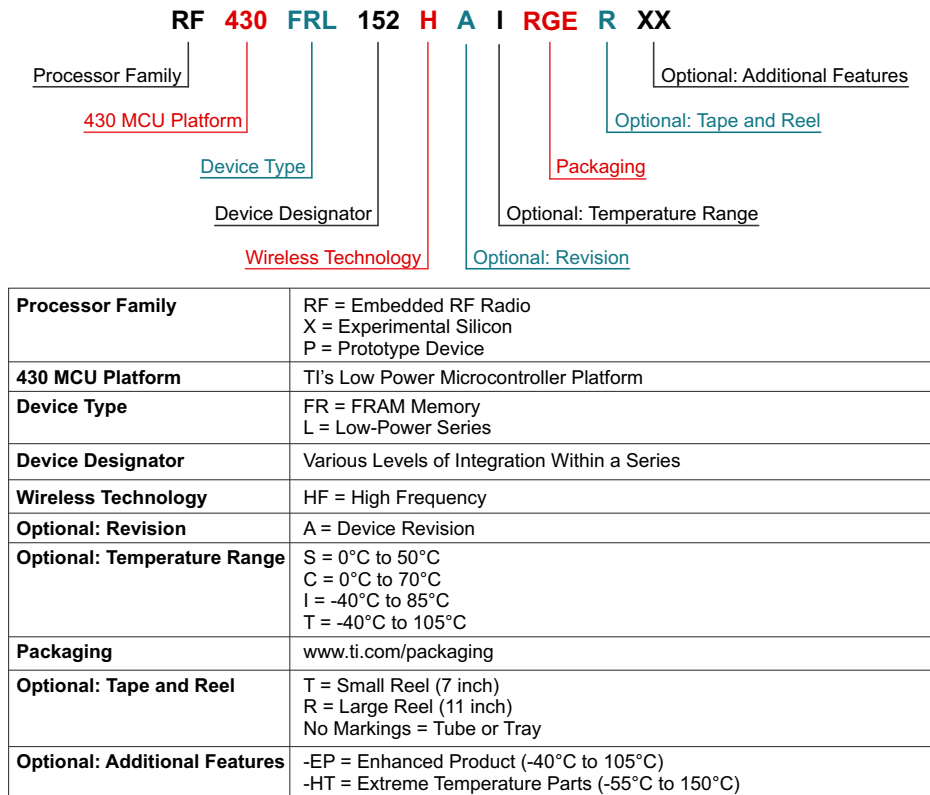


Figure 8-1. Device Nomenclature

8.2 Documentation Support

The following documents describe the RF430FRL15xH devices.

[SLAU506](#) *RF430FRL15xH Family Technical Reference Manual.* Detailed description of all modules and peripherals available in this device family.

[SLAU603](#) *RF430FRL15xH Firmware User's Guide.* Detailed description of the firmware that is provided for these devices.

8.3 Related Links

[Table 8-1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| RF430FRL152H | Click here | Click here | Click here | Click here | Click here |
| RF430FRL153H | Click here | Click here | Click here | Click here | Click here |
| RF430FRL154H | Click here | Click here | Click here | Click here | Click here |

8.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Community](#)

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#)

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.5 Trademarks

MSP430, Code Composer Studio, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical Packaging and Orderable Information

9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| RF430FRL152HCRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | RF430 FRL152H | Samples |
| RF430FRL152HCRGET | ACTIVE | VQFN | RGE | 24 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | RF430 FRL152H | Samples |
| RF430FRL153HCRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | RF430 FRL153H | Samples |
| RF430FRL154HCRGER | ACTIVE | VQFN | RGE | 24 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | RF430 FRL154H | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

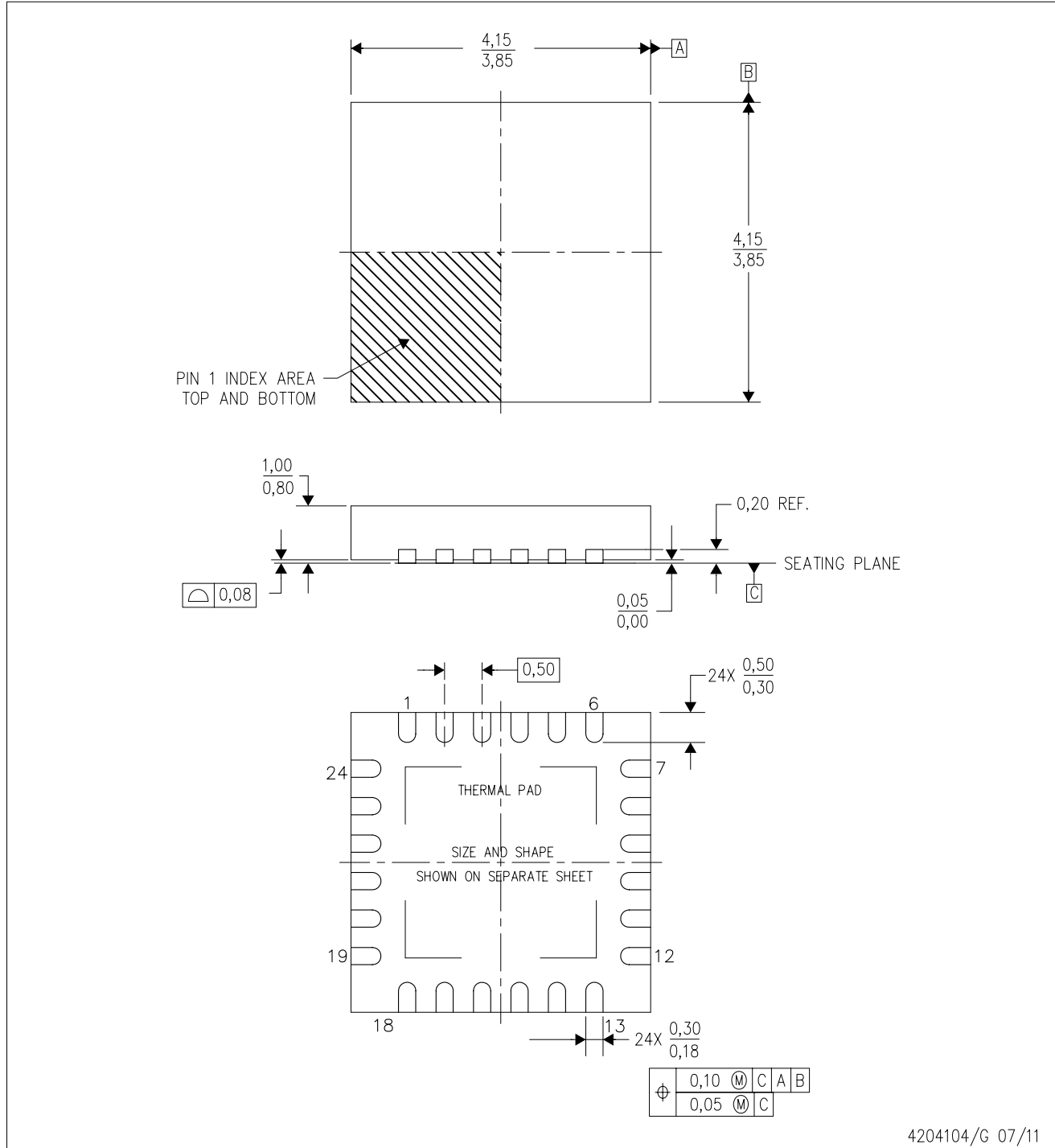
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



4204104/G 07/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Quad Flatpack, No-Leads (QFN) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

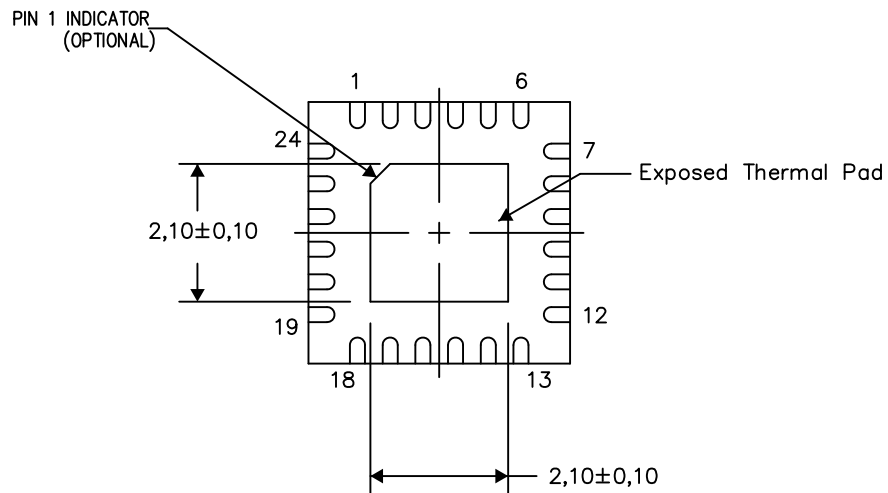
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

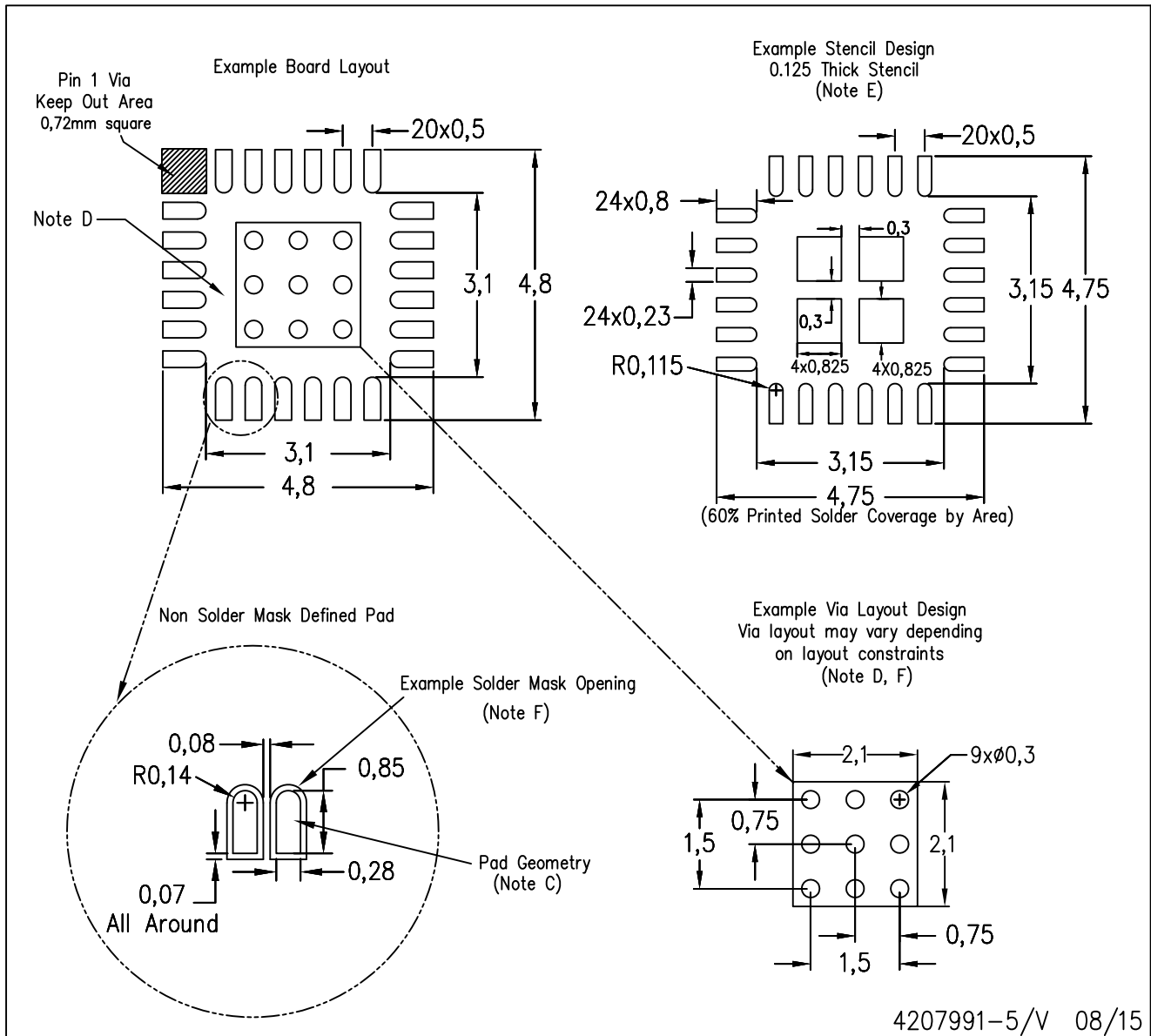
Exposed Thermal Pad Dimensions

4206344-7/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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